Master Thesis

DEVELOPMENT OF A MEASURING SYSTEM FOR THE ANALYSIS AND MONITORING OF ELECTROCHEMICAL CELLS AND STACKS

accomplished at

Master Degree Programme
Automation Technology - Economy

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Signature

EHRENWÖRTLICHE ERKLÄRUNG

Ich erkläre ehrenwörtlich, dass ich die vorliegende Arbeit selbstständig und ohne fremde Hilfe verfasst, andere als die angegebenen Quellen nicht benützt und die benutzten Quellen wörtlich zitiert sowie inhaltlich entnommene Stellen als solche kenntlich gemacht habe.

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DANKSAGUNG

Meine aufrichtigen Dankesworte gelten meiner Lebensgefährtin Olivia und meinen Stiefkindern Viola, Nina und Maya für ihre unermüdliche moralische Unterstützung sowohl während meines gesamten Studiums als auch während der Erstellung dieser Arbeit. Ebenso möchte ich meinen Eltern für ihre unerschütterliche Geduld und ihr Verständnis danken.

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Abschließend möchte ich der Band Black Sabbath danken, deren Musik mich während der Erstellung dieser Masterthesis begleitet hat.

KURZFASSUNG

Wasserstoff repräsentiert bereits heute eine bedeutende und vielfach eingesetzte Prozesschemikalie und wird als Sekundärenergieträger auch im großen Maßstab diskutiert. Die kontinuierliche Weiterentwicklung elektrochemischer Komponenten wie Elektrolyseure und Brennstoffzellen gewährleistet, dass sich Wasserstoff als nachhaltiger und erneuerbarer Sekundärenergieträger in zukünftigen Energieinfrastrukturen etablieren wird. Präzise Messmethoden, insbesondere die elektrochemische Impedanzspektroskopie (EIS), spielen eine entscheidende Rolle bei der Charakterisierung und Entwicklung. Trotz am Markt vorhandener EIS-basierter Messsysteme, erfüllen diese nicht immer alle Anforderungen der HyCentA Research GmbH. Das Hauptziel dieser Masterarbeit war die Überarbeitung eines EIS-Messgeräts, aus einem vorangegangenen Forschungsprojekte. Der Schaltplan des Prototyps wurde analysiert, modernisiert und um zusätzliche Funktionen erweitert. Der Messzweig, einschließlich Filter, Vorverstärker und Analog-Digital-Umsetzer (ADU), wurden überarbeitet. Ein grundlegendes Gerätekonzept wurde entwickelt, das Gehäuse, Anschlusstechnik und alle elektronischen Module umfasst. Ein Kalibrierungsverfahren und eine Betriebsstrategie für das Gesamtmessgerät, den "Zellmonitor", wurden ausgearbeitet. Die Umsetzung des Konzepts befindet sich derzeit in der Realisierungsphase, wobei der Zellmonitor dazu vorgesehen ist, sowohl in Prüfeinrichtungen als auch als mobiles Messgerät für Brennstoffzellenfahrzeuge zu dienen. Die zukünftige Anwendung des Zellmonitors trägt maßgeblich zur Fortentwicklung und Optimierung von wasserstoffbasierten Technologien bei.

ABSTRACT

Hydrogen currently serves as a significant and widely utilized process chemical and is also discussed as a big scale secondary energy carrier. The continual development of electrochemical components, such as electrolyzers and fuel cells, ensures that hydrogen is poised to establish itself as a sustainable and renewable secondary energy carrier within future energy grids. Precise measurement methods, particularly electrochemical impedance spectroscopy, play a pivotal role in characterization and development. Despite the existence of EIS-based measurement systems on the market, these do not consistently meet all the requirements set forth by HyCentA Research GmbH. The main goal of this thesis was the overhaul of an EIS measurement device which has been developed in a former research project The circuit diagram of the prototype was analysed, modernised, and expanded with additional functionalities. The measurement path, encompassing filters, preamplifiers, and ADC`s, was revised. A fundamental device concept was devised, including the housing, connection technology, and all electronic modules. Calibration procedures and an operational strategy for the overall measuring device, designated as the "Cell Monitor," were developed. The conceptual framework is presently in the process of implementation, with the Cell Monitor designed to serve in both testing facilities and as an onboard measuring device for fuel cell vehicles. The prospective application of the Cell Monitor significantly contributes to the advancement and optimization of hydrogen-based technologies.

TABLE OF CONTENTS

1 PROLOGUE

Perpetual change is an undeniable aspect of our existence, whether manifested through demographic shifts or alterations in societal structures. This dynamic is frequently instigated or expedited by technological advancements, often resulting in paradigm shifts. Presently, our society struggles predominantly with anthropogenic climate change. Efforts to mitigate this phenomenon extend beyond political and social measures to incorporate cutting-edge technological solutions. Over recent decades, numerous companies, startups, and academic institutions have committed to researching these technological imperatives, developing corresponding products, and bringing them to market. This endeavour encompasses not only novel technologies or recently discovered physical phenomena for energy conversion but also revisiting long-established technologies for this purpose.

Among the rediscovered technologies and energy sources, hydrogen stands out. Positioned as a potential energy carrier of the future, hydrogen finds versatile applications ranging from transportation to steel production. Functioning as a crucial process chemical, hydrogen has maintained its significance across various industries. The imperative for a sustainable hydrogen production, achieved through renewable energy sources, underscores the pivotal role of electrolysis plants, fuel cells, and hydrogen infrastructure components. In tandem with these core components, auxiliary systems, particularly in the domain of measurement technology, become indispensable for validating and verifying components such as electrolysis stacks.

This master's thesis establishes the basis for a measurement system, specifically an electronic measuring device. This device is designed for the measurement and monitoring of fuel cells and electrolysis stacks, it is able to measure precise and fast enough to execute EIS measurements. The collaborative effort between HyCentA Research GmbH and the Institute for Electrical Measurement and Signal analysis (EMS) at Graz University of Technology leverages a prototype developed by EMS, serving as the foundation for this thesis. The theoretical segment elucidates essential electrochemical principles, culminating in the derivation of electrical equivalent circuit diagrams, crucial for comprehending EIS functionality.[1]

Subsequently, a rudimentary model of the EIS measuring device, of the Cell Monitor is introduced to delineate the minimal prerequisites for such a device. In collaboration with EMS, the measurement-related criteria are defined. It has been determined, in addition to the specifications of the voltage monitoring, that additional high bandwidth current sensors need to be integrated. The conceptual framework is then refined, electronic modules are selected for incorporation into the cell monitor, and the circuit diagram of the measuring electronics undergoes analysis, leading to the development of an enhanced cell probe with additional functionalities. Emphasis is placed on ensuring compliance with measurement specifications. Finally, a basic calibration strategy is devised, guaranteeing the requisite measurement quality throughout all procedural steps.

[1] Translation assistance by ChatGPT.

2 PROBLEM DESCRIPTON

The main task is to develop a concept for a new cell monitor. This involves selecting electronic modules necessary for the operation of the cell monitor. This includes macro modules such as a computing unit like a single board computer and modules for the integration into a data network. The core module, the so-called “cell probe”, needs to be revised. The cell probe is the electronic assembly that records and digitises the measurement parameters acquired by the sensors that are required for an EIS. This involves revising the power supply concept as well as the measurement electronics and all circuit parts required for the operation of the new cell probe. Possible improvements should be identified and implemented. The result should be a revised circuit diagram and an overall device concept. Finally, a calibration concept should be developed to ensure the quality of the measurement results.

The research-leading question in this context is as follows.

“How can the development of a measuring device designed to facilitate the characterisation of fuel cells and electrolysers by electrochemical impedance spectroscopy be strategically optimised to ensure the precision and efficiency of measurements in this particular field?”

3 THESIS OVERVIEW

In section 4 “Theoretical fundamentals”, the fundamental functioning of fuel cells and electrolyzers is addressed, with a focus on elucidating the basic electrochemical principles. Electrical models are derived from these principles. Building upon this knowledge the operation parameters for EIS measurements are derived. These steps are necessary to both understand the measurement setup in which the cell monitor will be operated in the future, and to identify which measurement parameters need to be processed by the cell probe. Section 5 “Specifications” establishes the specifications of the cell monitor and the cell probe.

Chapter 6 “Applied sensor” deals with the sensors used to capture the measurement data. The Implementation begins in Chapter 7, starting with the definition of all modules of the cell monitor. The revision of the cell probe commences in Chapter 8 “Cell probe” and concludes with Chapter 9 “Calibration concept”, covering the calibration concept and the conclusion under chapter 10 summarizes the work done and discusses the additional steps required to turn the developed concept and schematic into a finished device. The following tools and resources were used to assist with the linguistic translations:

- Technical dictionary of TU Chemnitz
- ChatGPT
- Leo.org
- DeepL

If a paragraph or sentence has been translated using ChatGPT, it will be marked with a footnote in accordance with the citation style used at Campus02.

LTspice is used as the simulation software for electronic circuits as part of this thesis. It should be noted that the generated diagrams were also created with LTspice. The software does not allow changes to the labelling of the X and Y axes. In the case of AC analysis, where the X-axis represents the frequency in Hz, the unit prefix for kilo (kHz) is displayed with a capital "K," which should be lowercase. In the context of this work, it should be understood that KHz is intended to mean kHz.

In the case where a frequency response is presented with a different reference used as the output than the input quantity, this deviation is explicitly marked in the diagram.

4 THEORETICAL FUNDAMENTALS

In this chapter, the necessary electrochemical fundamentals and the functional principle of EIS are discussed. The knowledge gained from these insights serves as a foundation for the implementation. For this purpose, the topic of electrochemistry is considered as an introduction. On the one hand, the question of what constitutes electrochemistry is discussed, and on the other hand, how electrolysis and fuel cells function at a fundamental level. Based on these insights, electrical models of electrolysis and fuel cells are derived. Viewing electrolysis and fuel cells as electrical systems enables understanding of the functional mechanism. EIS measurements are applied to measure the aforementioned electrochemical components. Subsequently, the operation of EIS in terms of electronic processing is identified. The questions of how the measurement setup should be implemented, how the measured values are acquired, and finally, how the measured values are processed are clarified. Finally, all insights are summarized to derive measures for further processing.

4.1 A brief look at electrochemistry

Electrochemistry is a subdiscipline of physical chemistry. It combines the theory of electricity with chemical processes. It studies chemical phenomena at the contact surfaces between electronic conductors, called electrodes in this context, and an ionic medium, the electrolyte. More generally, electrochemistry studies the relationship between chemical and electrical energy. The boundaries with other disciplines such as electronics, materials science and solid-state physics are fluid.[2]

Findings from the field of electrochemistry are applied in a variety of processes and devices. Thus, also in electrolyzers and fuel cells. Different fuel cell and electrolysis technologies are also part of the research that is conducted at HyCentA.

4.1.1 Electrolysis in a nutshell

The fundamentals of water electrolysis are described based to the main part on literature.[3]

The electrochemical decomposition of water to produce hydrogen and oxygen is a state-of-the-art process. The underlying operating principle of hydrogen electrolysis is illustrated in Figure 1 on page 6. Two electrodes are placed in an electrolyte and connected with a Direct Current (DC) source.

The electrolyte is basically an aqueous solution. Acids such as HCL or bases such as KOH or water-soluble salts are added to the water to make the solution more conductive.[4]

As soon as a sufficiently voltage is applied to the cell, a redox reaction takes place in which hydrogen is produced, at the cathode (negative electrode) and oxygen at the anode (positive electrode).

[2] Cf. Kurzweil (2020), p. 3.

[3] Cf. Smolinka/Ojong/Garche (2015), p. 103 – 104.

[4] Cf. Klell/Eichlseder/Trattner (2018), p. 75.

The overall reaction of water decomposition is given by the stoichiometric equation (4.1).

$$2H_2O_{(l/g)} \Longrightarrow 2H_2 + O_2 \qquad (4.1)$$

Regarding to the supply voltage of the electrolyser, the following must be taken into consideration. Using the standard reaction enthalpy for electrolytic water splitting, the theoretically required voltage in the thermodynamic standard state can be determined. This is referred to as the decomposition voltage E_z and amounts to 1.48 V. To achieve a higher current flow and thus a higher gas yield, a higher voltage than the decomposition voltage must be applied. In the case of a forced current flow through the electrolytic cell, the voltage drop caused by the internal resistance R_i of the cell is added to the decomposition voltage. This results in the terminal voltage that must be applied through equation (4.2). From equation (4.2), it can be deduced that if current flow is desired, the applied voltage must be increased to initiate or enhance the electrolytic reaction. For deviations from the thermodynamic standard state, at least the so-called Nernst voltage E_n must be applied for water electrolysis. Starting from the Nernst voltage, the real decomposition voltage increases with increasing current flow due to losses caused by irreversible processes. This or a higher voltage must be applied so that electrolysis can occur. These additional voltages are referred as overvoltages. The required decomposition voltage is higher than the nominal voltage by the amount of ΔE, even without external current flow. This is due to diffusion processes, side reactions and charge losses.[5]

$$E_{cl} = E_Z + I \cdot R_i \qquad (4.2)$$

E_{cl}/V Terminal voltage

E_Z/V Decomposition voltage

I/A Cell current

R_i/Ω Internal resistance

Hydrogen electrolysis is an endothermic reaction that requires the input of energy. The two electrodes are immersed in a liquid electrolyte which allows ionic charge transfer to complete the external circuit via the DC power supply. In Figure 1(a), both gases migrate through the electrolyte and mix in the atmosphere above the electrolyte, forming explosive oxyhydrogen.

If the Electrolysis (EL) cell is to be used as hydrogen producer, the two half-cells must be separated to prevent the two gases from mixing and make the hydrogen and oxygen available, see Figure 1(b). In this case, a semipermeable diaphragm is used as a separator.

[5] Cf. Klell/Eichlseder/Trattner (2018) p. 74 – 78.

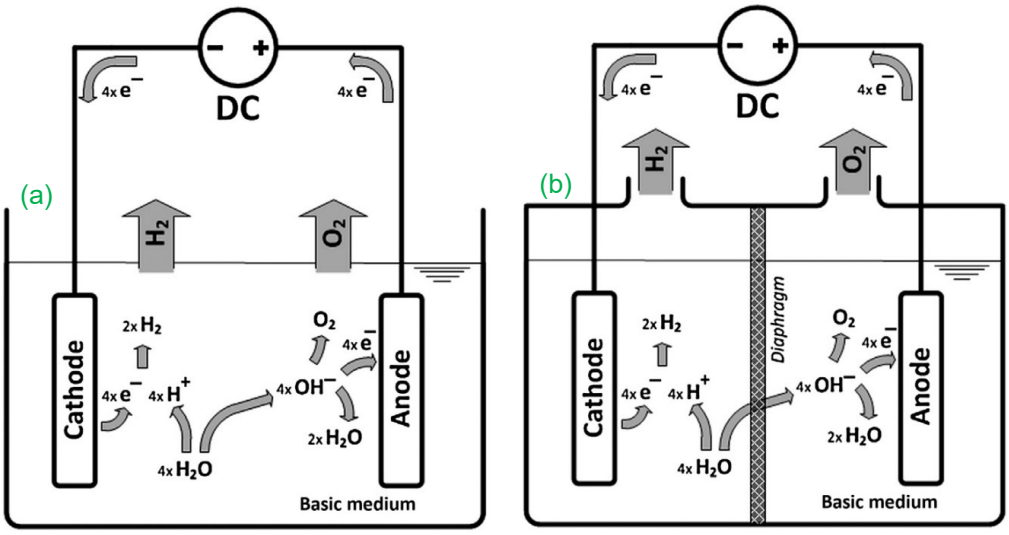


Figure 1: (a) Basic principle of an open EL cell in basic medium. The stoichiometric factors refer to the generation of an oxygen molecule. Since the half cells are open, oxyhydrogen gas is generated. (b) The use of a semi-permeable membrane between the two half-cells allows the separation of the two gases, source: Smolinka/Ojong/Garche (2015), p. 104 (slightly modified).

Various types of electrolytes can be used in an electrolysis cell. The Alkaline Electrolysis cell (AEL) uses a basic liquid electrolyte. In a Proton Exchange Membrane (PEM) EL cell, an acidic ionomer is used. In this case, the process is called Solid Polymer Electrolysis (SPE). The High Temperature (HT) EL cell has a solid oxide as the electrolyte. To ensure sufficiently high ionic conductivity, a minimum temperature is required for each electrolyte. The upper temperature limit is mainly determined by the stability of the cell materials and components.

4.1.2 Fuel cell in a nutshell

The explanations of the working principle of a Fuel Cell (FC) are taken from the literature.[6]

The operating principle of a fuel cell can be realized with different fuels and electrolytes. The fundamental operating principle of a fuel cell is explained based on a Hydrogen-Oxygen fuel cell (H2/O2 FC), or more precisely a Polymer Electrolyte Membrane Fuel Cell (PEMFC). The schematic structure of a PEMFC cell is shown in Figure 2. Hydrogen is supplied through the flow channels and diffuses through the gas diffusion layer to the anode (fuel or hydrogen electrode). The hydrogen is oxidized at the electrode with the aid of the catalyst to 2 H+ ions (protons), whereby two electrons are released. This process is called the Hydrogen Evolution Reaction (HER). These are absorbed and discharged by the anode, here the negative pole. The proton (H+) conducting polymer membrane, which is also the electrolyte, separates the two gas spaces from each other. Another property of the membrane is its insulating effect (electrical isolator) against the electrons. The protons are transported through the membrane to the cathode. In addition to the electrolyte structure, the proton conductivity of the membrane is mainly determined by the water saturation and the temperature. Since the electrons are not conducted through the membrane, they flow to the cathode via the external circuit due to the potential difference. In the process, work is

[6] Cf. Klell/Eichlseder/Trattner (2018) p. 145 – 146.

performed in a connected load. The oxidizing agent (electron acceptor) oxygen is in turn fed to the electrode of the cathode (oxygen electrode) via the flow channels and the gas diffusion layer. At the cathode, with the help of the catalyst, the oxygen is reduced (Oxygen Evolution Reaction (OER)) by accepting the electrons and combines with two protons to form a water molecule (product water). The product water diffuses via the gas diffusion layer into the flow channels, where it is discharged from the cell with the flow.

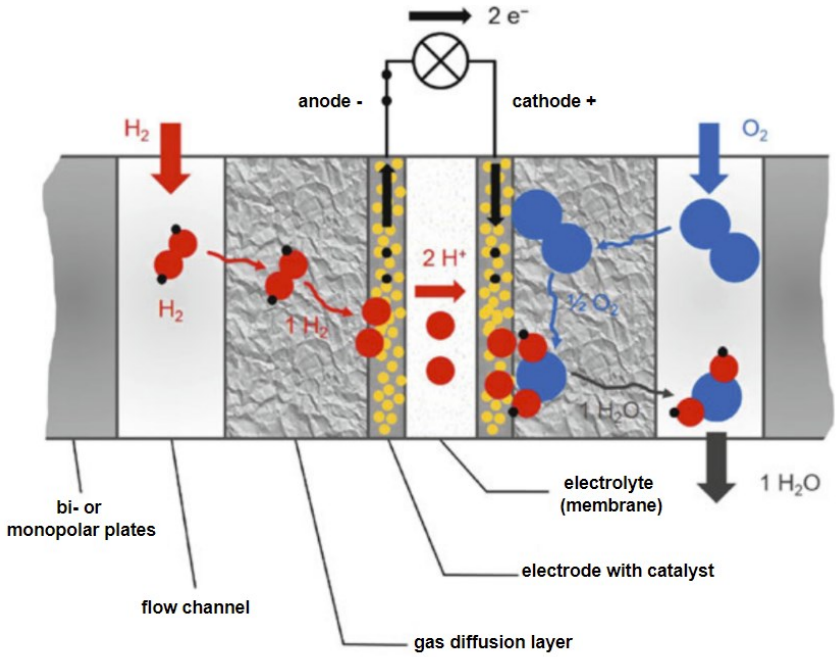


Figure 2: Principle of a PEMFC fuel cell, source: Klell/Eichlseder/Trattner (2018), p. 145 translated.

4.2 The method of electrochemical impedance spectroscopy

With EIS, parameters of electrochemical cells can be measured and characterized, such as the resistance of an electrolyte or the effects of different materials. This measurement method can be applied to any electrochemical component, such as an electrolysis cell or stack. The measurement results provide information about its condition and cell parameters, for instance the conductivity of the electrolyte, or the polarisation resistance of the ongoing electrochemical reactions in the measured cell.

EIS is used to measure the impedance of the Device Under Test (DUT). Two different measurement methods are applied. In the potentiostatic method, a specific operating voltage is applied to the DUT, resulting in a corresponding current flow through the specimen. In contrast, in the galvanostatic method, a specific current is applied to the test specimen, resulting in a corresponding voltage across the DUT. Both measurement methods can be applied for the assessment of both electrolyzers and fuel cells. Since an electrolyzer is operated with direct current in normal operation and the fuel cell is a direct current source, an alternating current or voltage must be superimposed on the operating current or voltage in an EIS measurement. This allows the impedance of the test object to be measured.[7]

[7] Cf. Kurzweil (2020) p. 102.

Figure 3 illustrates this relationship using a potentiostatic measured electrolytic cell. An exemplary U/I-curve, in this context, it is also referred as a polarization curve, of an arbitrary electrolytic cell is created. The voltage in volts is plotted along the X-axis. The point U_{BIAS} represents a stationary operating point of a DC voltage applied to the test specimen. Along the Y-axis, the resulting current is plotted in amperes. The point I_{BIAS} stands for the resulting current which occurs at U_{BIAS}. In the EIS, a sinusoidal excitation signal (blue) is now imposed. The excitation signal is a frequency-variable signal with a known amplitude. The imprinting of the excitation signal is manifested in the current system response (red signal).

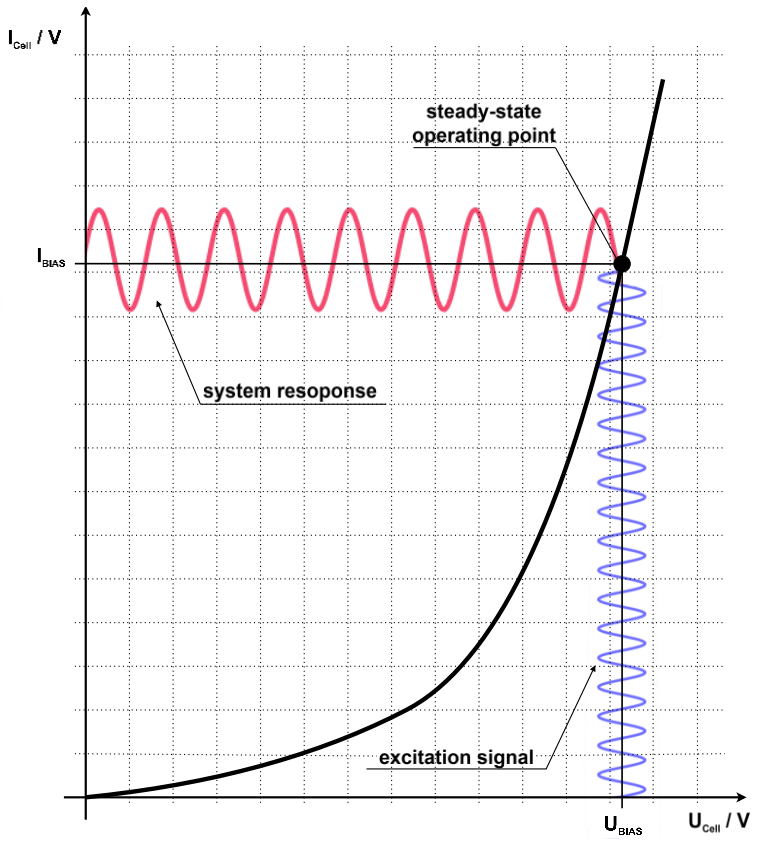


Figure 3: U/I curve of an electrolysis cell operated with potentiostatic impedance method, source: based on Kurzweil (2020), p. 102.

The impedance spectrum is acquired from high frequencies to low frequencies. The generated excitation signals vary in the frequency spectrum from multiple kHz to mHz which are applied to the test object. In order to calculate the corresponding impedances, the respective amplitude and the phase shift φ between current response and voltage response must be measured for each frequency step. Figure 4 shows the phase shift between current and voltage using two exemplary sinusoidal signals. The amplitude can be read along the Y-axis.[8]

[8] Translation assistance by ChatGPT.

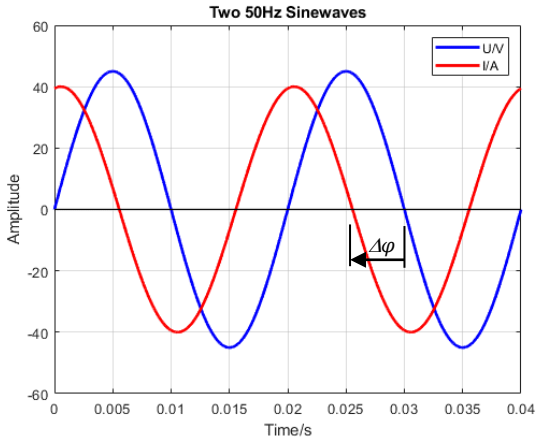


Figure 4: Phase shift and amplitudes of two sinusoidal signals, source: self-created.

Subsequently, signal multiplication and averaging are used to separate the useful signal from the DC components, harmonics and noise. Frequency response analyzers output the complex resistance $\underline{Z}$ or impedance magnitude and phase (Z, φ).[9]

More precisely, the impedance is calculated from the current and voltage spectrum using a Fourier transformation according to equation (4.3).

$$\underline{Z}(j\omega) = \frac{\mathcal{F}\{U(t)\}}{\mathcal{F}\{I(t)\}} = \frac{\int_{-\infty}^{\infty} u(t) \cdot e^{-i\omega t} dt}{\int_{-\infty}^{\infty} i(t) \cdot e^{-i\omega t} dt} \qquad (4.3)$$

$\underline{Z}$/Ω	Impedance
$\mathcal{F}$	Fourier transform
I/A	Current
U/V	Voltage
ω/s^{-1}	harmonic frequency
t/s	Time

The corresponding impedance is calculated for each frequency. There are two fundamental graphical representations to visualize the calculated data. On the one hand the Nyquist plot and on the other hand the Bode plot. A negative value on the imaginary axis indicates capacitive behaviour. Electrolyzers and fuel cells typically exhibit capacitive behaviour at measured frequencies. It is common to display the Bode and Nyquist diagrams together in a 3D plot, where the negative imaginary axis is flipped and visualized as a **positive** axis.[10]

Figure 5 illustrates an exemplary 3D plot. Here Z' corresponds to the real part and Z'' to the imaginary part of the impedance of the electrochemical cell. Beneath Figure 5a) the magnitude is plotted versus the frequency. Under b) is the Nyquist plot. Finally, the phase response is plotted under c). The result of all plots is an area in the three-dimensional space. It can be observed that the magnitude and the Nyquist

[9] Cf. Kurzweil (2020) p. 102.

[10] Cf. Lasia (2014) p. 48 – 49.

plot are projections of the three-dimensional impedance plot. The progression of the impedance along the area d corresponds to the phase response.

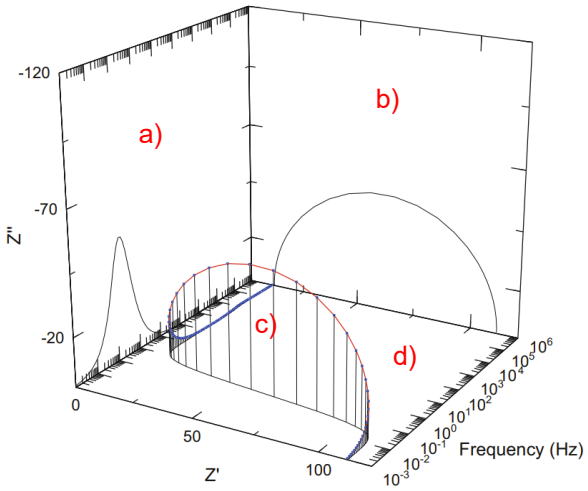


Figure 5: Example of a three-dimensional impedance plot source: based on an illustration of Lasia (2014), p. 50.

The Nyquist diagram of the impedance in the complex plane shows semicircular arcs due to the capacitive behaviour of the DUT's. Irreversible electrode processes act like ohmic resistors *R*, limiting the flowing current and releasing waste heat, for example the breakdown reaction. Reversible electrode processes act like capacitive reactance X_c, for example the double layer recharge. The capacitance *C(ω)* maps the activity of the electrode surface. At higher frequencies, the electrolyte resistance and the double layer capacitance are measured.[11]

Finally, it is worth mentioning that, in the real implementation, the nyquist sampling theorem must be taken into consideration. The theorem implies that the signal to be measured must be sampled with at least twice its frequency. Furthermore, instead of the continuous Fourier transformation, the so-called discrete Fourier transformation should be applied, since in reality an ADC digitizes the analog signals and only discrete data can be obtained.

4.2.1 System-theoretical consideration of electrochemical cells

For a more profound understanding of the electrical behaviour, this chapter discusses the development of a foundational electrical model for both the fuel cell and the electrolysis cell. In the initial phase, general system-theoretic assumptions are formulated. To further examine the operation of an EIS, an equivalent circuit diagram for the electrochemical cell is introduced. This involves considering an electrolysis stack based on proton exchange membrane technology.

In order to derive cell-related parameters from the impedance spectrum and the associated graphical interpretation, a model fitting is required. The applied model for a PEM electrolysis single cell is shown in Figure 6. A PEM electrolyzer is constructed in a stack structure. This stack comprises a series connection of multiple individual single cells. Each individual single cell consists of a membrane, an anode side, and

[11] Cf. Kurzweil (2020) p. 103.

a cathode side surrounded by so-called bipolar plates. A detailed description can be found in Chapter 6.1. To apply this model, it must be assumed that the device under test is a linear time invariant system (LTI). To ensure this, the amplitude of the excitation signal must be kept as low as possible.[12] Due to the small amplitude of the excitation signal, the nonlinearity of the DUT has a minimal effect and can thus be linearized.

Only by assuming that the DUT is an LTI system, the equivalent circuit shown in Figure 6 can be used as a model-fit circuit. Since the model-fit-circuit itself represents an LTI system.

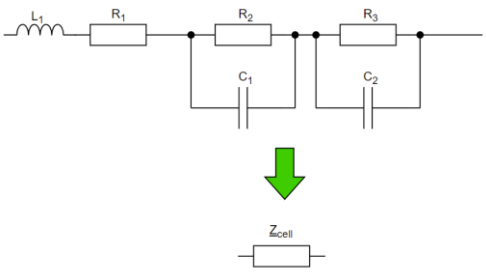


Figure 6: Electrical model of the impedance of a PEM electrolysis single cell, source: based on Eder (2022), p. 43.

Figure 7 shows that if the amplitude of the U/I characteristic is sufficiently small, the linearisation error can be kept low, consequently the system property of linearity applies in this working range. The points $\hat{U}_{INT+}$ and $\hat{U}_{INT-}$ on the X-axis represent the maximum and minimum amplitude of the excitation signal. The pink marked area shows the value range of the excitation signal and the system response. Analogous to the excitation signal, the minimum $\hat{I}_{INT-}$ and the maximum $\hat{I}_{INT+}$ of the amplitude of the system response were plotted on the Y-axis.

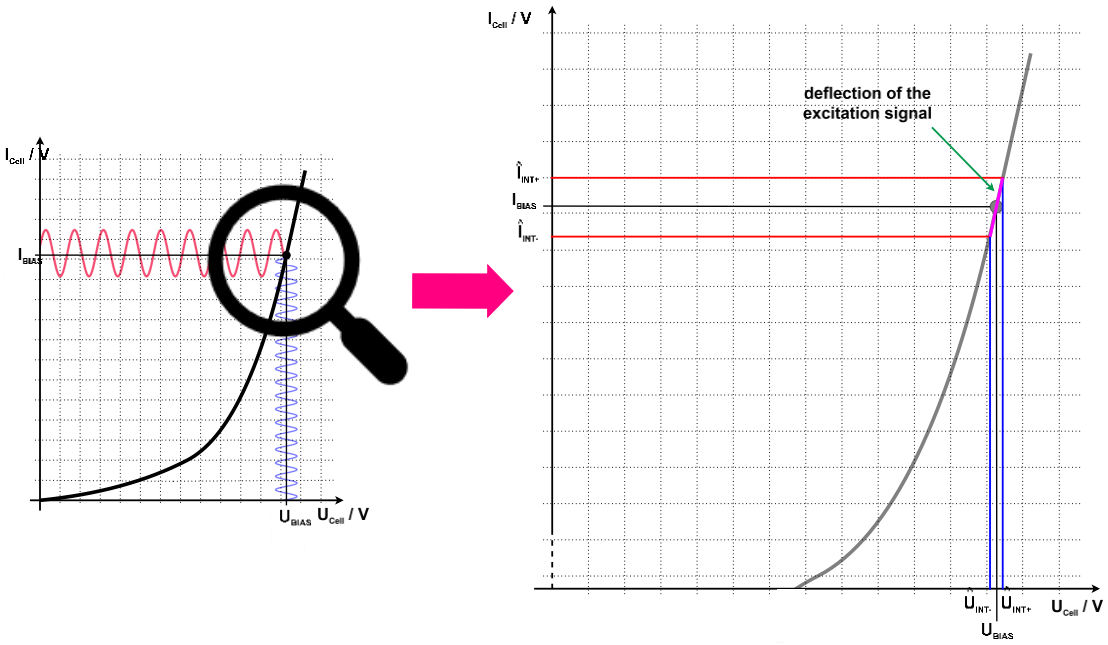


Figure 7: Linear section of the U/I characteristics, source: self-created.

[12] Cf. Eder (2022) p. 22.

Regarding time invariance, it is important to consider that such an assumption is valid only when the test duration is limited to the shortest possible period. In other words, it should be kept as short as possible to ensure the assumed system property of time invariance. Prolonged test durations could potentially induce alterations or degradations in cell chemistry, thereby casting doubt on the assumption of temporal invariance. This methodology is not only applicable to various types of fuel cells or electrolyzers but can also be extrapolated to other types of electrochemical cells, such as lithium-ion accumulators, necessitating corresponding adjustments to the modelling circuits.

4.2.2 Equivalent electrical circuit

In electrical engineering, an electrolysis cell can be interpreted as a complex impedance corresponding to a load. The impedance is the AC resistance. In the case that an electrolyzer is operated with direct current, only the effective component, the ohmic resistance manifests within the impedance. A fuel cell, in simplified terms, converts supplied hydrogen into electrical power, acting as a voltage source capable of generating a defined voltage and the resulting current. To illustrate, Figure 8 depicts the equivalent circuit diagram for both an electrolysis cell and a fuel cell under steady-state and normal operating conditions. In the normal operation of an electrolysis cell, a constant direct current with a constant direct voltage is applied to the cell. For a fuel cell, normal operation entails maintaining input parameters, such as hydrogen supply, constant, resulting in the generation of a constant direct current.

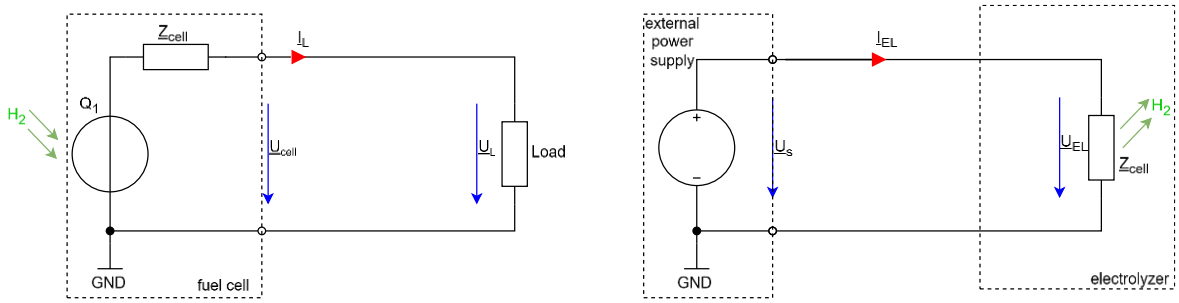


Figure 8: On the left, the fuel cell's equivalent circuit diagram in normal operation with the load connected, on the right, the equivalent circuit diagram of the electrolysis cell with an external voltage source, source: self-created.

To gain a better understanding of the system, a simulated switch-on attempt will be conducted at this point. During switch-on and switch-off scenarios, transient phenomena arise, primarily attributable to impedance effects. To illustrate the switch-on process, a simulation of an electrolysis cell was applied. In this simulation, the general impedance Z_{cell} was substituted with a fit model, and parameters were designated for each individual component. The switching dynamics of the switch S were then simulated utilizing the prescribed parameters. This simulation approach is directly applicable to the fuel cell by employing its respective impedance model.

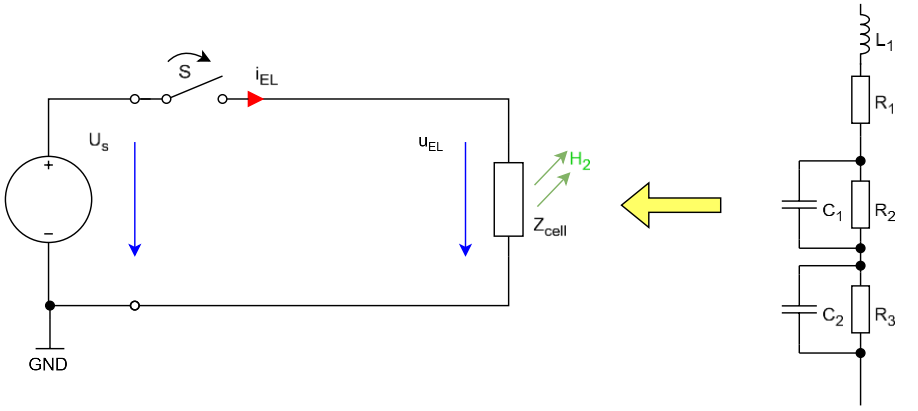


Figure 9: Circuit diagram of the transient process, source: self-created.

The simulation results for an electrolysis cell are depicted in Figure 10, Figure 11, and Figure 12, with the component values based on real parameters derived through a model fit for the model of the single cell impedance from Figure 9.[13] The internal resistance of the external voltage source was neglected, and all components were treated as ideal. At the voltage source V1, an additional 1.02 V overvoltage was applied to the 1.48 V. The value of 2.5 V for a single cell is a common value in practice for single cell testing. Figure 10 presents the simulation circuit in LTspice. As shown in the diagrams of Figures Figure 11 and Figure 12, the transient process takes place over approximately 2 µs. Within this timeframe, changes in current flow through L1, C1, and C2 become visible. Subsequently, a stable current flow occurs through L1 and the resistors (R1, R2, and R3). Due to the fact that capacitors act as infinite resistances for direct currents, no further current flows through them after the transient process.

This simulation illustrates that a disturbance variable necessary for EIS measurements causes the impedance of capacitors C1 and C2 to decrease with increasing frequency, while the current through the capacitors increases accordingly. In contrast, with increasing frequency, the impedance of inductor L1 increases. With further increasing frequency, the impedance at L1 would become so large that the measurement current would be blocked by the DUT, and the Nyquist plot would exhibit a purely inductive behaviour. Consequently, an upper limit for EIS measurements owing to the excitation signal frequency is established.

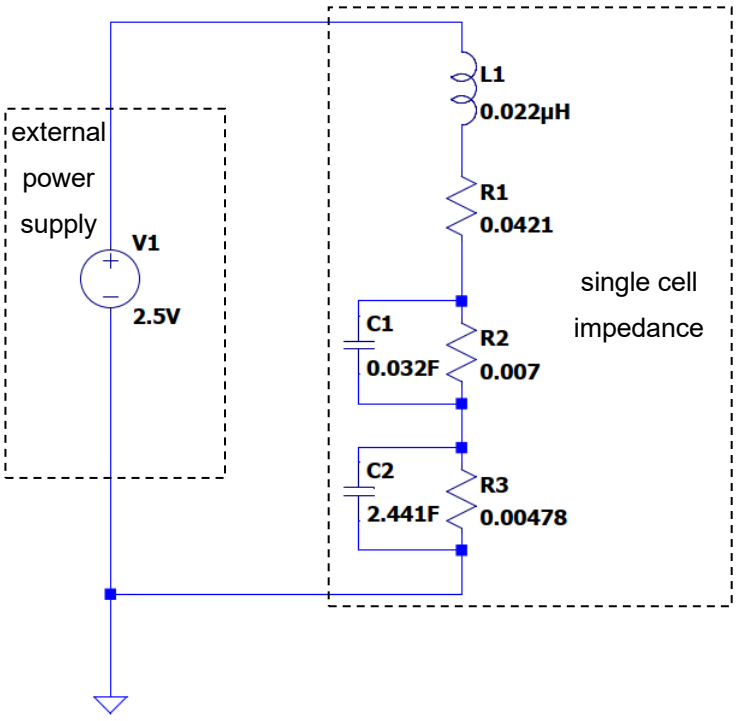


Figure 10: Simulation circuit of a single-cell electrolyser operated at an external voltage source with real model fit parameters, Source: self-created.

[13] Cf. Eder (2022) p. 45.

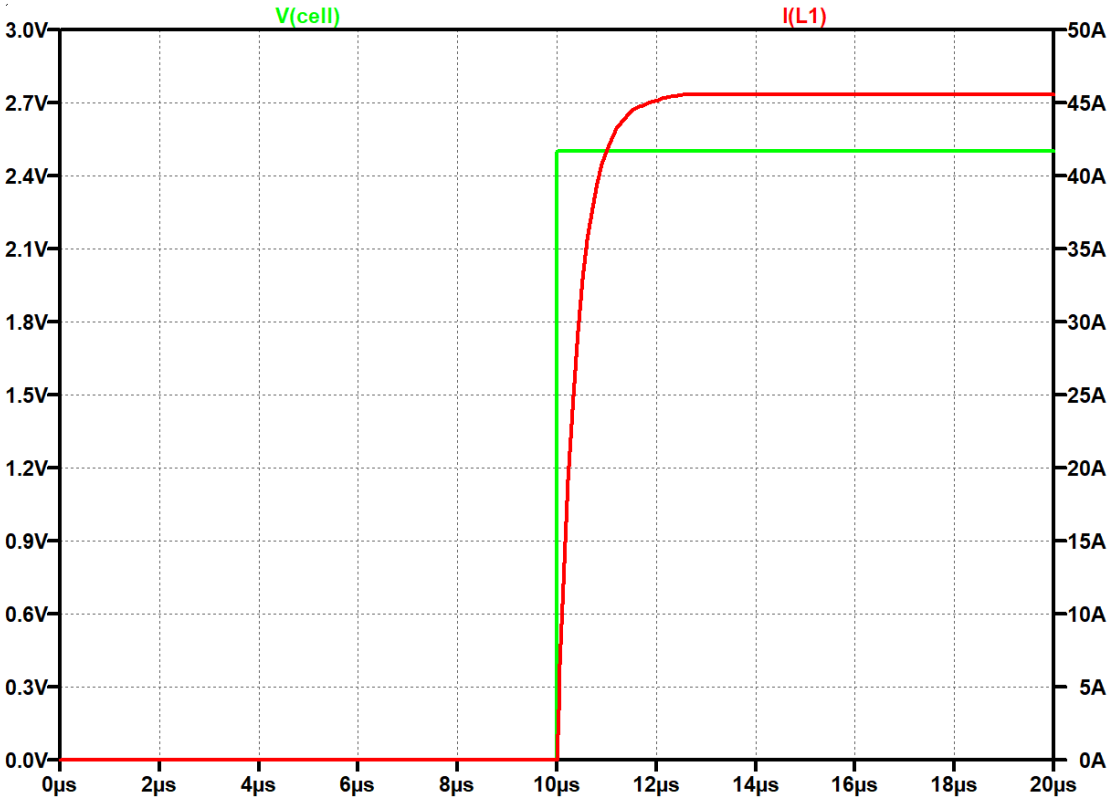


Figure 11: Transient current flow through the inductance L1, source: self-created.

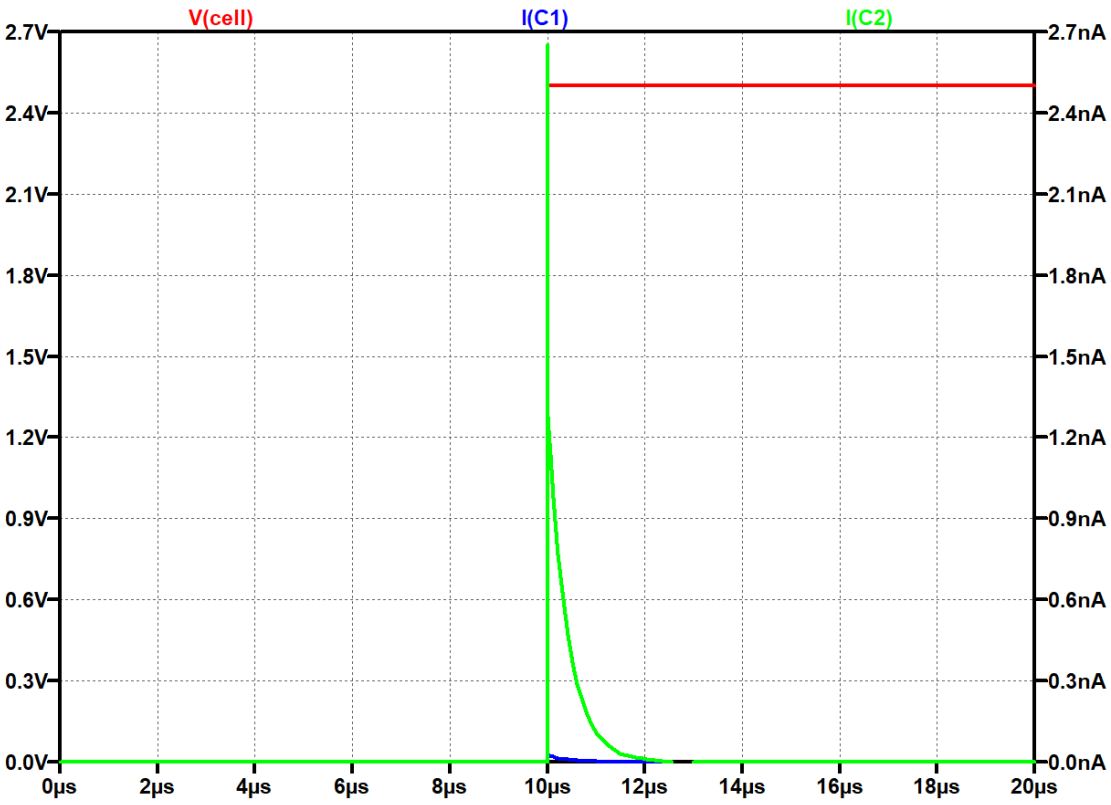


Figure 12:Transient current flow through capacitor C1 (blue) and capacitor C2 (red) L1, source: self-created.

If the fuel cell and electrolysis cell are measured via EIS (see 4.2 page 7), the initial situation changes as follows.

At this point, for instance, the electrolysis cell is measured in galvanostatic mode. Figure 13.b illustrates the voltage curve of the cell voltage U_{cell} over time. The excitation voltage U_{EX} is generated by the excitation current I_{EX} and coupled to the operating voltage. The operating voltage represents the voltage of the operating point U_{BIAS}. From the perspective of the electrolysis cell, the modulated excitation current I_{EX} leads to a modulated cell voltage U_{cell}, which increases or decreases hydrogen production by the amplitude of the current. Figure 13.d demonstrates how the sinusoidally modulated load affects the operating current I_{BIAS} of the fuel cell. The modulation generates an alternating current termed I_{INT}. The operating current I_{BIAS} is accordingly only attenuated. The operating current I_{BIAS} is not exceeded. A controlled exceeding of the operating current by an additional source would mean that this source would feed the fuel cell itself. This, in turn, would disrupt the chemical process that converts hydrogen into electricity. In the case of a PEM-based fuel cell, feedback would imply that hydrogen would be produced at the anode during the time when the current from an additional source is higher than the current supplied by the fuel cell. This could lead to damage to the fuel cell and must therefore be avoided.

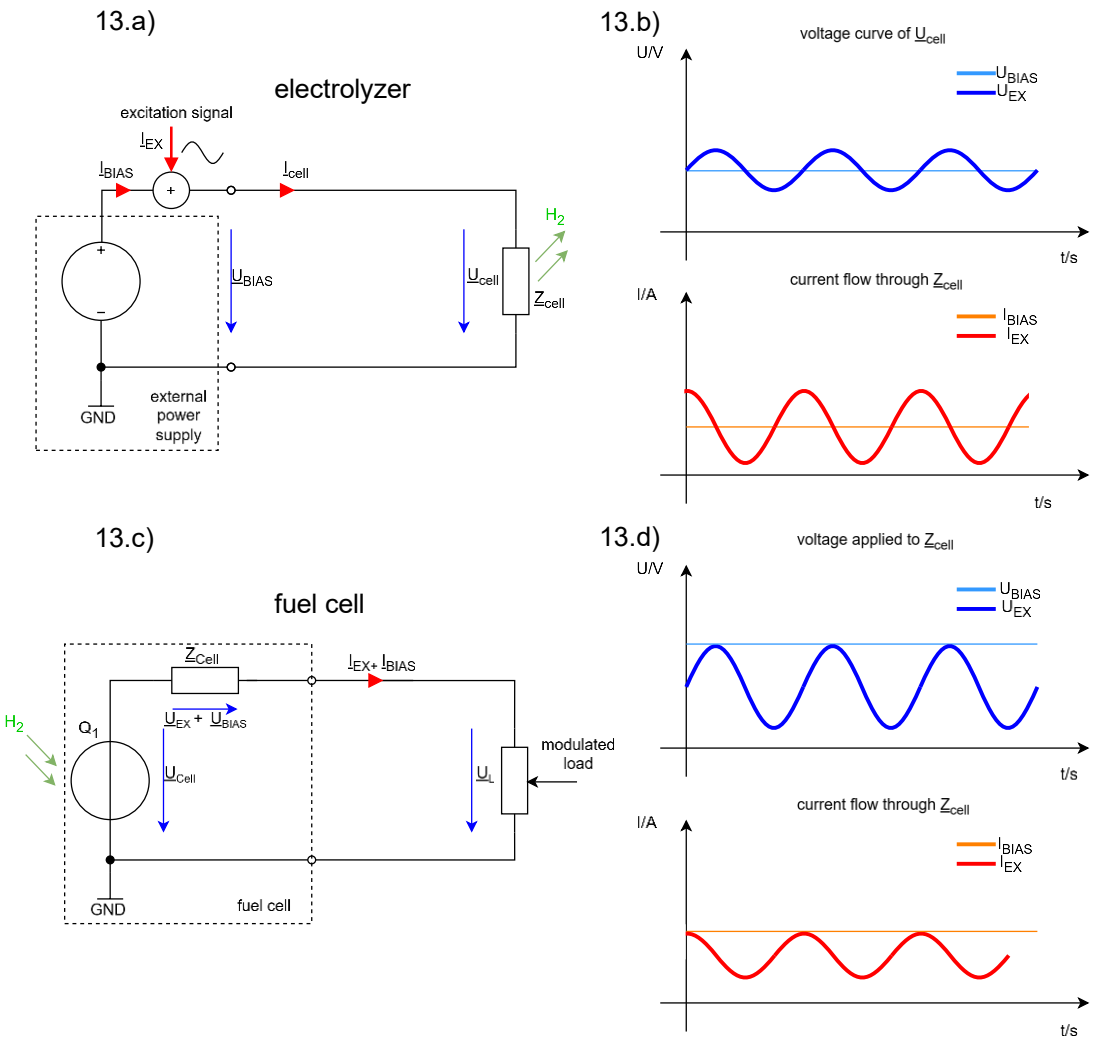


Figure 13: Circuit diagram of an electrolysis cell in potentiostatic measurement mode (top), circuit diagram of a fuel cell at a modulated load (bottom), Source: self-created.

4.2.3 Voltage evaluation in electrolysis cells under current

The following chapter evaluates the voltage that is established at the individual cell when a current is specified. For this purpose, the voltage source (see Section 4.2.2, Figure 10) was replaced by a constant current source, and an AC analysis was conducted. The frequency was increased logarithmically from 0.1 Hz to 100 kHz, and a current with an amplitude of 1 A was applied. This allows the voltage of the simulation result to be interpreted as a percentage. A Bode diagram was created where the voltage U_{cell} is plotted linearly along the Y-axis.

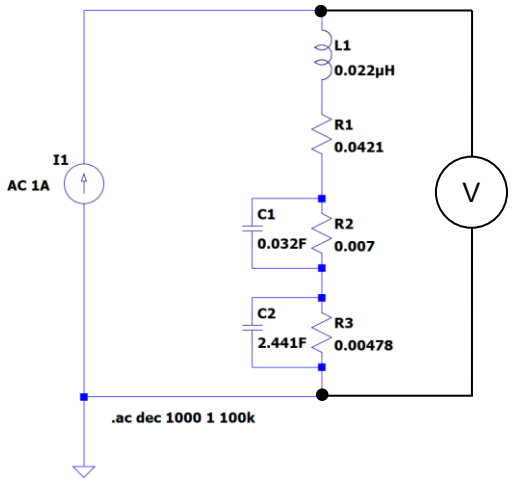


Figure 14: Adapted simulation circuit, source: own illustration.

In Figure 15, the simulation result is depicted. At 0.1 Hz, the voltage is approximately 54.9 mV, which only slightly increases up to 100 kHz. From 10 kHz onwards, the influence of inductance gradually increases, causing the overall impedance to rise. However, this implies that with increasing frequency, the cell's equivalent circuit behaves inductively and significantly reduces the measurement current, making further analysis of capacitance and resistance impractical. The relationship between the applied measurement current and the generated alternating voltage across the cell is 0.0549 % of the applied current, approximately 1:18. This ratio depends on the component parameters, but this simulation result serves to determine the magnitude of the voltage to be measured.

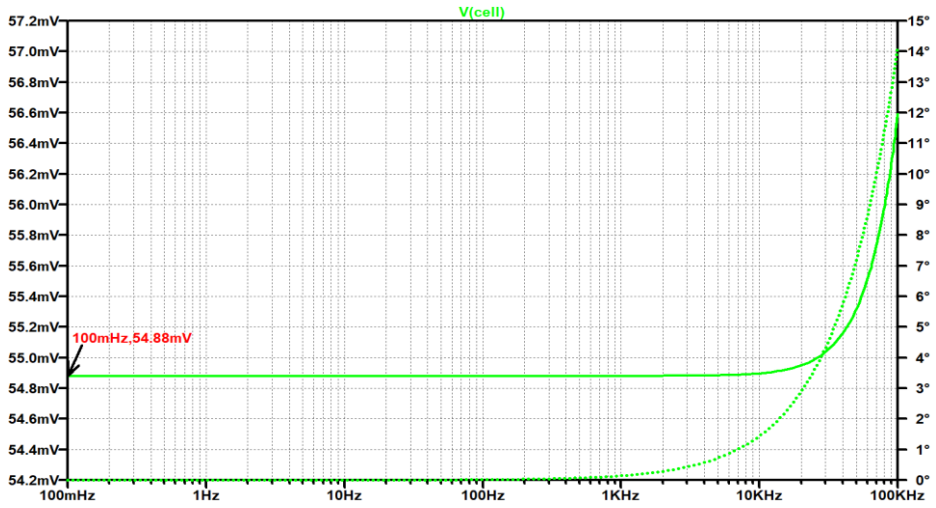


Figure 15: Frequency and amplitude response of the cell voltage within the simulation circuit, source: own illustration.

4.2.4 Measurement circuit

A specialized measurement apparatus essential for employing EIS is termed a cell monitor. This device records the voltages and currents applied to the device under test across all frequencies. Figure 16 illustrates the integration of a cell monitor into the measurement setup for potentiostatic measurement of an electrolytic cell or stack. The electrolysis cell or stack, symbolized by $\underline{Z}_{cell}$, is linked to a voltage supply that imposes the operating DC voltage ($\underline{U}_{BIAS}$). This voltage is overlaid with an excitation voltage ($\underline{U}_{EX}$). Both voltage sources are under the control of an Electronic Control Unit (ECU), which regulates the frequency and amplitude of the excitation voltage $\underline{U}_{EX}$. On the DUT side, the cell monitor samples the cell current ($\underline{I}_{cell}$) and the voltage ($\underline{U}_{cell}$) across the DUT.

For the measurement setup involving a fuel cell, distinctions arise due to the fuel cell functioning as a voltage source. Similar to the electrolysis cell, the fuel cell is controlled by an ECU. However, a load with modulation capabilities is necessary. The cell monitor measures the load current ($\underline{I}_L$) flowing through the internal impedance of the fuel cell and the modulated load. Simultaneously, the cell voltage (U_{cell}) of the fuel cell is measured. The modulation of the load affects both the frequency and the amplitude of $\underline{I}_L$.

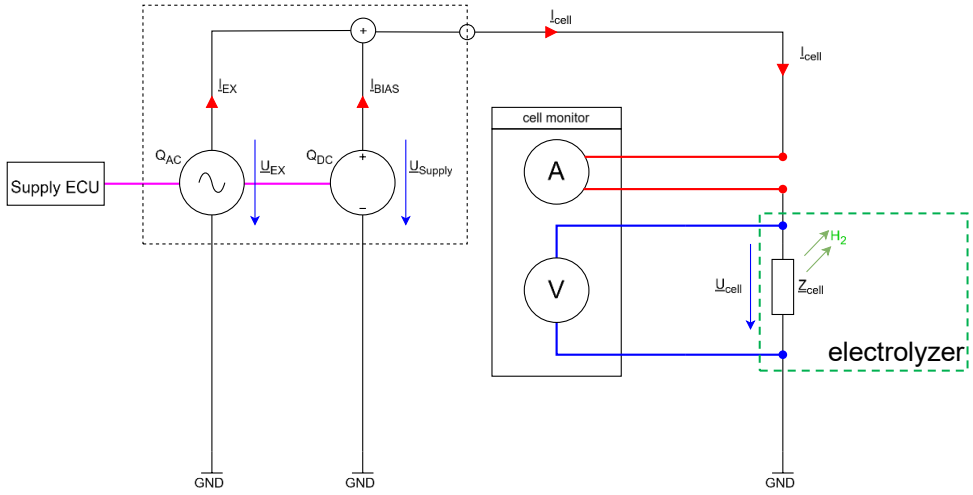


Figure 16: Measurement setup of an electrolysis cell or stack with integrated cell monitor, source: self-created.

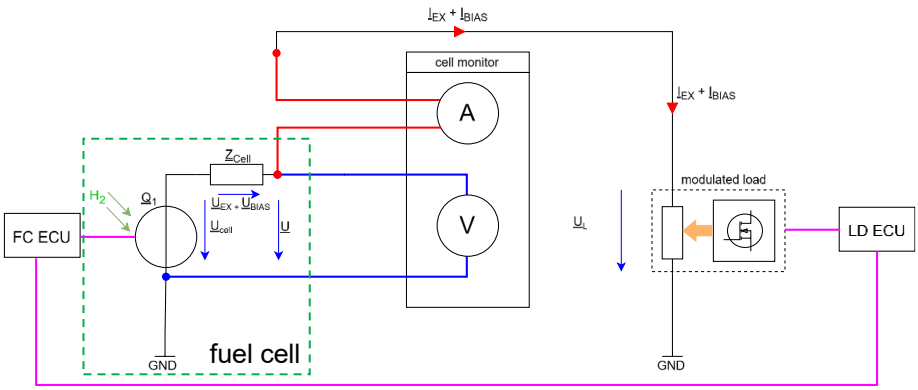


Figure 17: Measurement setup of a fuel cell with integrated cell monitor, source: self-created.

5 SPECIFICATIONS

The following specifications have been prepared together with experts from the EMS as well as the HyCentA Research GmbH. All requirements for the cell probe were summarized and presented in tabular form in chapter 5.2.

5.1 Modular structure of the entire system

The complete measurement system comprises a single board computer (SBC), the aforementioned cell probe, and a data network module. It incorporates all essential interfaces along with their corresponding connectors. Within the housing, an Ethernet switch serves as the data network module. A controller area network (CAN) interface is integrated to facilitate communication with external components, such as an electronic control unit (ECU) for fuel cell regulation or a power supply unit. The CAN interface also enables control over a DC-DC converter, employed as a modulable load for fuel cell measurements. The CAN interface is implemented using a USB to CAN converter directly connected to the SBC. Facilitating data exchange between the SBC and the cell probe, both modules are equipped with Ethernet interfaces. Optionally, a host computer can be linked via Ethernet for additional functionalities if needed. This optional host computer can supplement or replace the function of the SBC. Basically, the cell monitor can be controlled with the host computer. The measurement signal post processing and algorithm development can also be implemented on the host computer. As already mentioned, the activities described above can also be carried out on the integrated SBC. The main function of the SBC is to store or buffer the measurement data and execute the EIS evaluation via digital signal processing algorithms. The cell probe represents the measurement electronics. On the cell probe, the current and voltage values captured by the sensors are digitised by an ADC. The quality parameters of the measuring channels specified in the requirements are strictly adhered to. There are two channels on the cell probe, one for voltage measurement and the other for current measurement. The voltage can be tapped using the specially provided connections on the bipolar plates of the individual cells, also called the Cell Voltage Monitoring (CVM) connections. In order to be able to measure the stack voltage, measuring connections are extruded on stack current collectors and main connection plates. Figure 18 shows a block diagram of the Cell monitor.

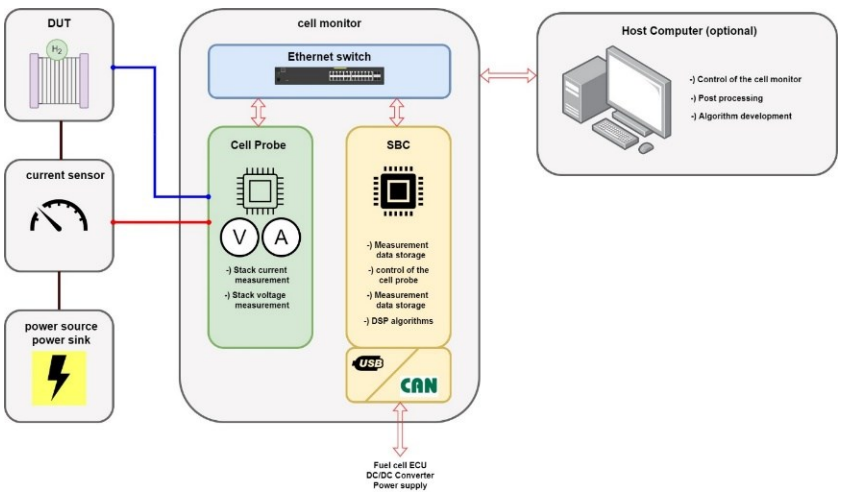


Figure 18: Modular design of the entire measuring system in which the cell probe is used. Source: self-created.

5.2 Requirements

In the following table, all the requirements for the cell probe board are summarized. All specified parameters were determined by the project partners at HyCentA Research GmbH and the EMS.

Cell probe requirements					
Signal processing and supply					
Modul	Category	Characteristics	Symbol	Rating	Unit
power supply	General:	Input voltage	U_{in}	24 (9 to 36 tolerant)	V
Voltage measurement	DC voltage measurement:	Voltage range	VR_{V1}	max 1000	V
		Resolution	R_{V1}	16	Bit
		Analog signal bandwidth	f_{BWV1}	max 25	kHz
		Signal to noise ratio	SNR_V	100 (FS)	dB
	AC decpoupling:	Corner frequency	f_{CV}	0.1	Hz
		Voltage range	VR_{V2}	+/- 10	V
		Resolution	R_{V2}	16	Bit
		Sampling rate	DR_{V2}	min 50	kS/s
		Analog signal bandwidth	f_{BWV2}	max 25	kHz
Current measurement	General:	Input range current signal	I_{isig}	+/- 667	mA
	Sensor power supply:	Supply voltage	U_{sens}	+/- 15	V
		Output current	I_{sens}	1.1	A
	AC and DC current characteristics:	Resolution	R_{I1}	16	Bit
		Analog bandwidth	f_{BWI1}	min 25	kHz
		Signal to noise ratio	SNR_I	100 (FS)	dB
		Corner frequency	f_{CI}	0.1	Hz
Additional functions					
Type		Functions			
Internal online self-calibration (IOSC):		-) Offset correction -) Gain correction -) Voltage to current gain missmatch -) Voltage to current phase missmatch			
Operating conditions					
Type		Rating		Unit	
Ambient temperature		-20 to 60		°C	
Enclosure (Water ingress and foreign body intrusion)		min. IP54		---	
Connectivity					
Purpose		Specification			
Power supply connection		Min. of power requirement and corresponding ip code			
Voltage sensor connector		SUB-D 9			
Current sensor connector		SUB-D 9			
CAN (ECU communication)		SUB-D 9			
Ethernet (Host computer com.)		RJ45			
USB (Firmware programming)		USB C			

Table 1: Table of requirements regarding cell probe board, source: self-created.

6 APPLIED SENSOR

In the following sections, an evaluation of the sensor technology used in the entire measurement setup is conducted, encompassing both the cell monitor and its peripheral devices. Section 6.1 addresses the voltage measurement, while section 6.2 deals with the types of current sensors used.

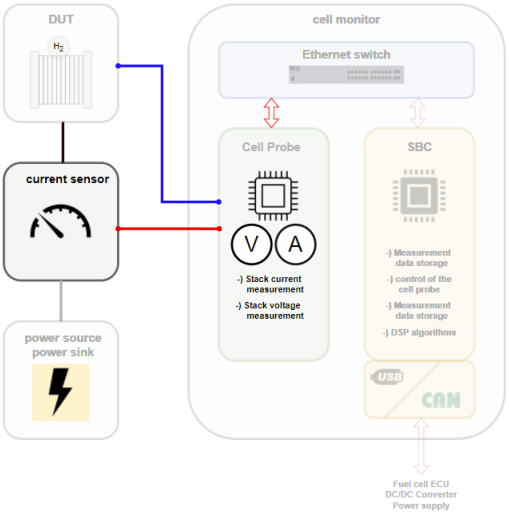


Figure 19: Measuring setup with the focus on the sensors source: self-created.

6.1 Voltage measurement

The integration of the voltage measurement into a test specimen is demonstrated using a PEM electrolyser.

Essential to the concept is the membrane material Nafion (sulfonated tetrafluoroethylene polymer). The Nafion membrane combines the functions of a diaphragm and proton-conducting electrolyte. The cells only need to be supplied with deionised water. The addition of acidic or alkaline agents to increase conductivity is not necessary. Figure 20 shows the schematically structure of a PEM electrolysis cell. The hydrogen cation (H+) conducting membrane is directly connected to the electrodes. This component is called membrane electrode assembly (MEA). The MEA is connected to the bipolar plates via porous current conductors (gas diffusion layer) and is permeable to the product gases and water. The end plates of the cell contacts the current source. In addition, they contain the flow channels for the transport of liquid water to the anode, the removal of oxygen from the anode and the removal of product hydrogen from the cathode.[14]

[14] Cf. Klell/Eichlseder/Trattner (2018) p. 83 – 84.

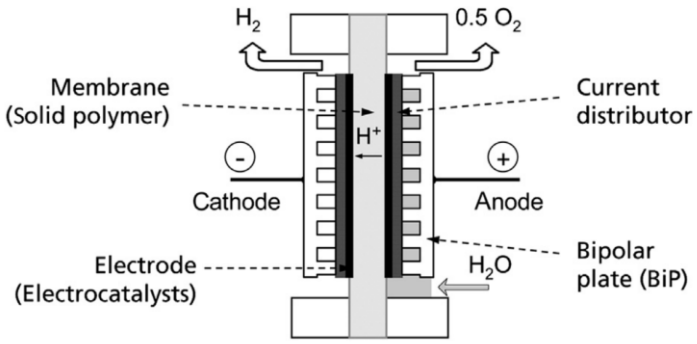


Figure 20: Simplified schematic of a PEM electrolysis cell, source: (Smolinka/Ojong/Garche 2015, p. 115).

Several PEM single cells can be connected to form a so-called stack. A stack represents the combination of several cells connected in series, which increase the total effective cell area and thus achieve a high electrical connected load. The layer pattern shown in Figure 21 is reproduced in the stack.[15]

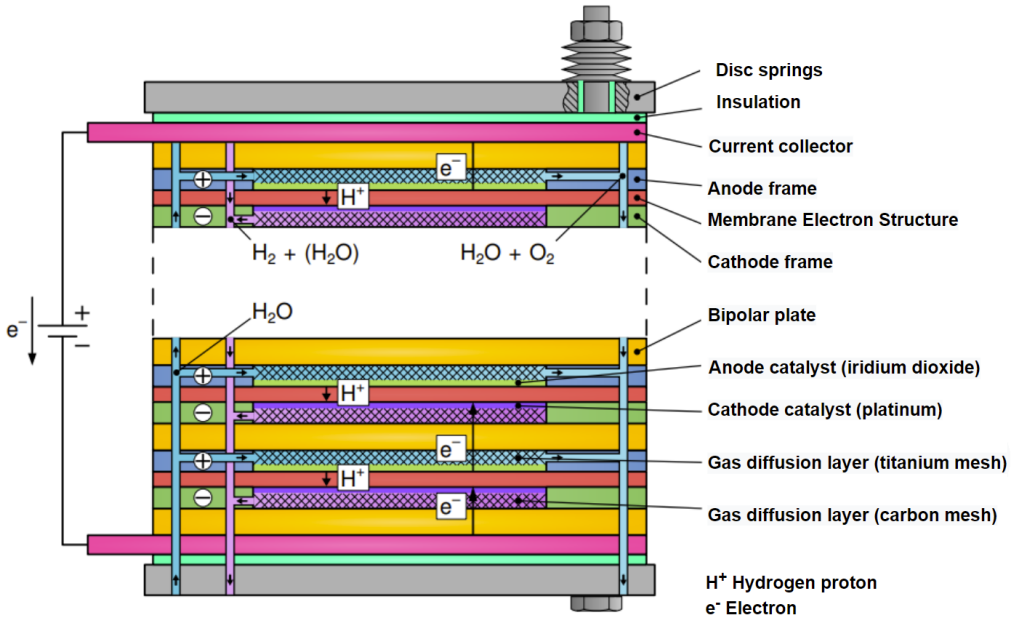


Figure 21: Exemplary PEM stack structure, source: adapted from Weiskopf (2023), p. 12.

The voltage supply is established via the current collector or at specially provided connections on the bipolar plates of a single cell or a partial stack. These connections are also used for voltage measurement.

Figure 22 shows a PEMEL stack with the aforementioned connections for the power supply. The current collector connection can also be seen. The second current collector connection is located between the lower base plate and the first cell pack. This is connected directly via the base plate. This applies analogously to PEM fuel cells. However, the converted electrical power is provided at the terminals.[16]

[15] Cf. Weiskopf (2023) p. 12 – 13.

[16] Translation assistance by ChatGPT.

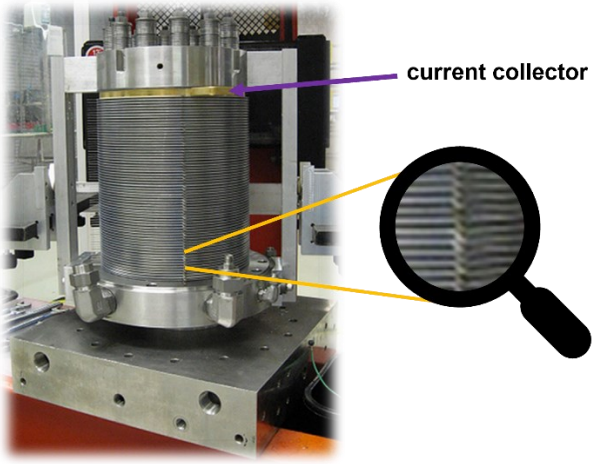


Figure 22: PEMEL stack with connections for the power supply, source: adopted from Berger/Wolf/Rieder (2018), p. 118.

Applying a 4-wire measurement according to Figure 23, the current is fed into the impedance $\underline{Z}_{cell}$ to be determined via two leads and the voltage is tapped via $\underline{Z}_{cell}$ with two separate leads. The voltage measuring terminals are directly connected to the impedance $\underline{Z}_{cell}$. This contacting ensures that the unavoidable voltage drops via the power supply lines $\underline{Z}_{w1}$ and $\underline{Z}_{w2}$ are not included in the voltage measurement. In addition, the voltage measurement lines are almost current less due to the high internal resistance of the voltmeter, so that no or only a very low voltage drops at the voltage measurement contacts and the lines $\underline{Z}_{v1}$ and $\underline{Z}_{v2}$. The measured voltage therefore corresponds very exactly to the voltage at the impedance $\underline{Z}_{cell}$. As a result, the voltage drops at the contact and line resistances of the power supply lines are not recorded because of the separate contacting and the contact resistances of the voltage measurement lines are negligible because of the internal resistance of the voltmeter.[17]

To compensate for the phase shift caused by the measurement leads, known impedance cables such as coaxial cables are used. Additionally, a reference measurement can be performed with a known impedance. By calculating the difference between the reference measurement and the measurement on the DUT, the influence of the measurement leads can be determined and compensated for.

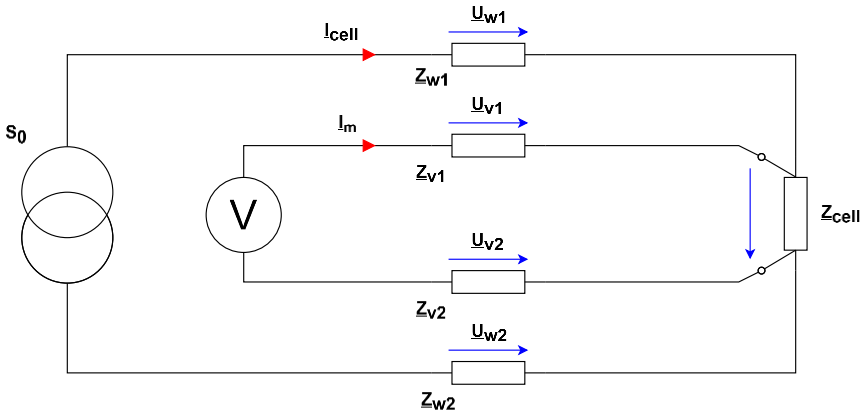


Figure 23: Rudimentary circuit diagram for four-wire technique, source: self-created.

[17] Cf. Mühl (2012) p. 130 – 131.

$\underline{Z}_{cell}$ of Figure 23 symbolizes an electrochemical cell such as a PEM electrolysis stack. Figure 24 shows the implementation of the four-wire technique on the basis of a schematic PEM electrolysis stack where, as mentioned in the previous section, the voltage can be connected to the current collectors and/or to the bipolar plates of individual cells. The greenish yellow plates symbolize the current collectors and their connections, the dark gray plates represent the bipolar plates including their measurement connections.

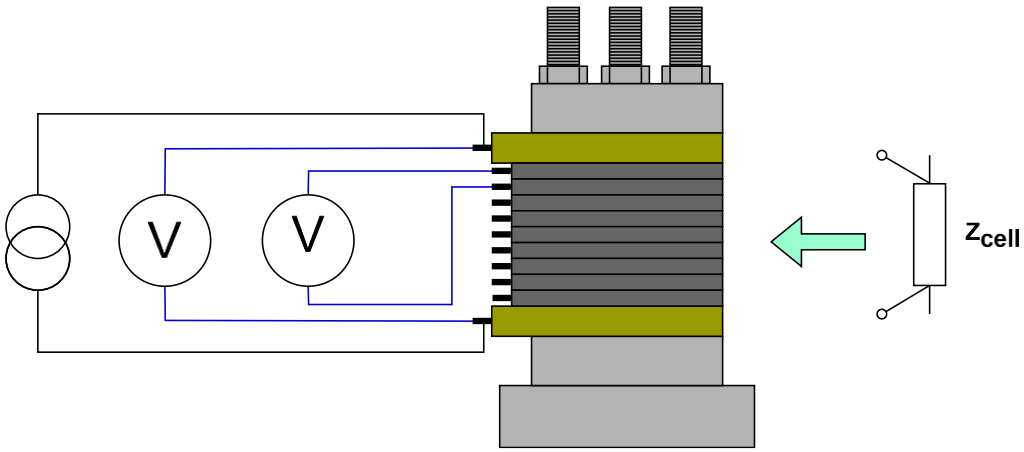


Figure 24: Four wire measurement shown on a schematic of a PEM electrolysis stack, source: self-created.

6.2 Current measurement

Shunt resistors are not used as current sensors for the cell monitor. The reason is that shunt resistors cannot be electrically isolated without additional effort, and the measurement circuit must be opened to integrate the shunt resistor. This makes this measurement method impractical for use with the cell monitor in a test setup. Furthermore, shunt resistors are less robust against overloads compared to fluxgate current sensors, which can be caused by errors in the experimental setup. Additionally, the currents occurring in the test operation are high (up to 1000 A), which increases the costs for shunt resistors in this measurement range.

Galvanically isolated current transformers with an air core can measure AC or pulsed DC currents, but not pure DC currents. Therefore, galvanically isolated current transformers with an air core are not an option.[18]

Due to their moderate bandwidth, response time, and temperature sensitivity compared to other sensor types, open-loop Hall sensors are not suitable. Closed-loop Hall-effect sensors, on the other hand, offer similar advantages to fluxgate current sensors, such as contactless and galvanically isolated measurement of AC and DC currents.

[18] Cf. LEM Components (2006), Online-Quelle [28.10.2023] p. 36.

The negligible offset of the fluxgate current sensor results in high accuracy. Since high measurement accuracy over the entire range is desired, fluxgate technology is used in the measurement setup.[19] There are a large number of types and manufacturers on the market. For the most part, fluxgate sensors, like other sensor technologies, have standardized current and voltage interfaces, making their integration into measurement setups easier. Their functionality is described below. Both current-supplying and voltage-supplying types can be operated on the cell monitor.[20]

Figure 29 shows the basic structure of a standard fluxgate sensor. The application of the measuring principle of the fluxgate sensor requires a soft magnetic iron core. Similar to hall sensors, the fluxgate probe is located in an air gap of the iron core. In addition, a symmetrical evaluation unit and an amplifier are used for operation. The so-called compensation coil is also located on the iron core.

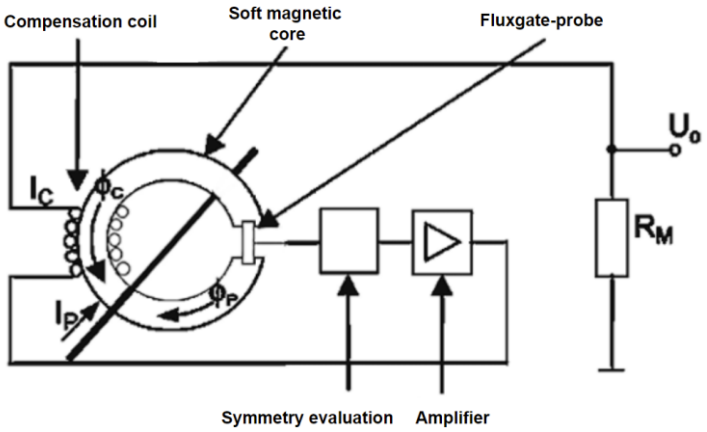


Figure 25: Schematic structure of a fluxgate current sensor, source: adapted from (Berger/Wolf/Rieder 2018, p.131).

When a current-carrying conductor (I_P) is passed through the toroidal core, I_P causes a magnetic flux in the core. The conductor can be considered as a coil with one turn (N_P=1). This magnetic flux is measured by the fluxgate probe. The core of the fluxgate probe consists of a soft magnetic, highly permeable material with three surrounding coils of copper wire. The magnetisation characteristic of the fluxgate probe shows the dependence of the flux density on the magnetic field strength. The magnetisation characteristic of the fluxgate probe is point-symmetrical to the origin as long as no external magnetic field is present. Figure 26 shows an exemplary magnetisation characteristic curve.[21]

The magnetisation characteristic curve shows the relationship between the magnetic field strength *H* and the magnetic flux density *B* of a magnetisable material. The magnetic field strength *H* can be regarded as a localised magnetic excitation which generates the magnetic flux density *B* under the influence of the material. With regard to the influence of the material, it should be mentioned that ferromagnetic materials already have an order of the atomic magnetic fields for small areas, the so-called Weiss domains. The effect of external magnetic fields leads to a uniform alignment of the Weiss domains, which considerably strengthens the magnetic field, but also explains the appearance of magnetic saturation. Figure 26 shows

[19] Cf. LEM LEM Components (2006), Online-Quelle [28.10.2023] p. 30

[20] Translation assistance by ChatGPT.

[21] Cf. Berger/Wolf/Rieder (2018) p.131.

the so-called initial magnetization curve (black line with red arrows) The initial magnetization curve is the relationship between the magnetic field strength and the magnetic flux density *B* during the initial magnetisation of a completely demagnetised material. (H = 0 Am^{-1}, B = 0 Vsm^{-2}).

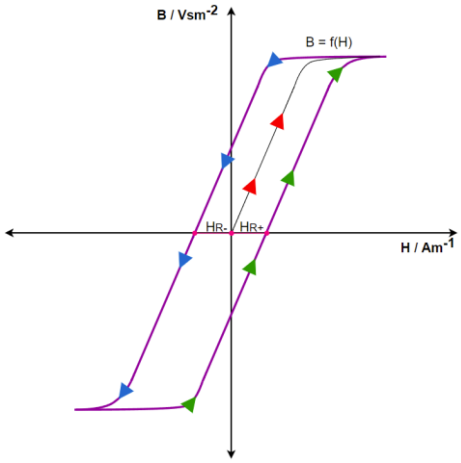


Figure 26: An exemplary magnetisation characteristic curve, source: self-created.

The application of an external magnetic field in addition to the internal magnetic field leads to the generation of a magnetic flux density *B*, which first appears hesitantly and becomes steeper with increasing field strength and finally barely increases at all (saturation region). The hysteresis (purple curve) occurs during cyclic magnetic field reversal. It is noticeable that the graph does not pass through the origin. This is due to the so-called magnetic remanence. The remanence phenomenon can also be explained by the effect of the weiss domains The remanence represents a permanent magnetisation of the material. As soon as a coercive field strength is reached (e.g., H_{R-}), a certain part of the Weiss domains remains permanently aligned. This permanent alignment results in the aforementioned remanence.[22]

The fluxgate probe is connected as a cantilever oscillator, whereby the coil is energised in such a way that the core is saturated alternately in both directions. The result is a rectangular output signal whose duty cycle is depending on an external H-field.[23] Figure 27 shows the fundamental structure of a fluxgate probe.

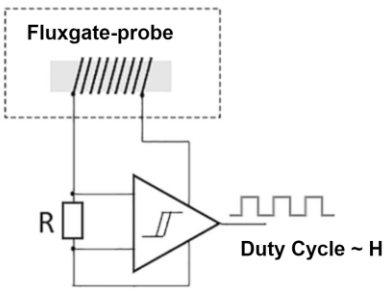


Figure 27: Structure of the fluxgate probe: Soft magnetic core with enclosing coil, source: adapted from Berger/Wolf/Rieder (2018), p. 131.

[22] Cf. Zastrow (2018) p. 191 – 192.

[23] Cf. Berger/Wolf/Rieder (2018) p. 131.

The fluxgate probe is supplied with a square-wave voltage. When the current drawn from the voltage source flows through the coil of the fluxgate probe and reaches a certain threshold value, the polarity of the applied voltage is reversed. This happens periodically. In the steep area of the B-H curve (magnetisation characteristic), the inductance of the fluxgate probe is orders of magnitude higher than the inductance in the saturation area of the core material (areas with a low gradient). When saturation is reached in the core material, the coil current increases rapidly. The polarity of the voltage applied to the coil is reversed as soon as the predefined current threshold is reached.[24]

This is used to generate an output signal that is proportional to the strength of the external magnetic field. This is achieved by the periodic modulation of the magnetic field, which drives the magnetic material of the sensor in and out of saturation. The resulting changes in the magnetic flux are measured and output as a signal from the sensor. The amplitude of this signal therefore directly corresponds to the intensity of the external magnetic field acting on the sensor.

Figure 28 a) shows the structure of an abstracted fluxgate current sensor. The fluxgate probe is located in the air gap of the iron core which is also surrounded by the compensating coil. In the absence of an external magnetic field, the iron core of the fluxgate probe itself is magnetised by source current I_1. This results in a magnetisation characteristic curve shown in Figure 28 b).

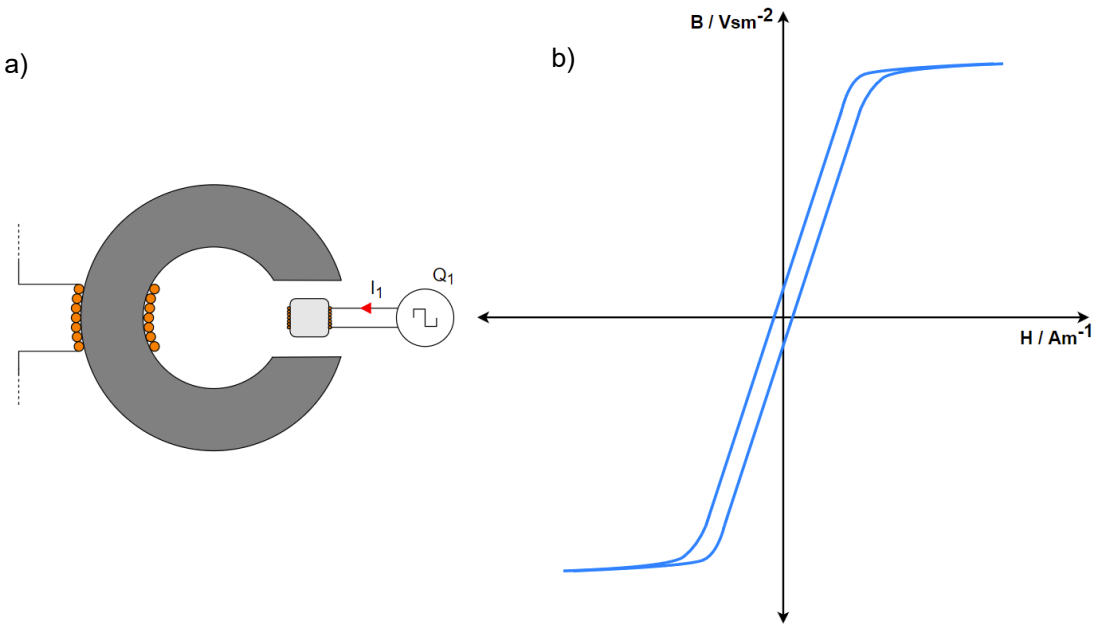


Figure 28: Abstract structure of the fluxgate current sensor with an exemplary magnetisation characteristic curve without external magnetic field, source: self-created.

When a conductor is placed through the iron core of the fluxgate sensor which carries the current I_P, an H-field is generated in the iron core of the sensor. The resulting magnetic flux φ_p closes over the air gap in

[24] Cf. Berger/Wolf/Rieder (2018) p. 132.

which the fluxgate sensor is located. This creates an asymmetry in the magnetisation characteristic of the iron core of the fluxgate probe. The hysteresis graph is shifted along the H-axis.[25]

Figure 29 a) shows the same fluxgate sensor as in Figure 28 a) with a current-carrying conductor passed through it. The current Ip results in the flux φ_P through the outer iron core. As already mentioned, this closes via the air gap. The magnetic flux φ_P generated by I_P flows through the iron core of the fluxgate probe which is located in the air gap and interferes with the existing magnetic flux generated by the current I_1 of the voltage source Q_1. If you look at the magnetisation characteristic curve, you can see that the additional magnetic flux φ_P is added to the existing magnetic field strength as an additional magnetic field strength or subtracted from it.

The increase in the field strength also results in an increase in the magnetic flux density *B*. Figure 29 b) shows a magnetisation characteristic curve. H_P corresponds to the magnitude of the magnetic field strength resulting from the magnetic flux φ_P. The magnetic flux density B_P is added to the field strength. The arrow (dark blue) indicates that the flux flows through the iron core of the fluxgate probe in such a way that it reaches positive saturation. The pair of values H_P and B_P mark the new starting point. this means that the path to positive saturation, which must be travelled on the graph, is longer than to saturation on the negative coordinate section.

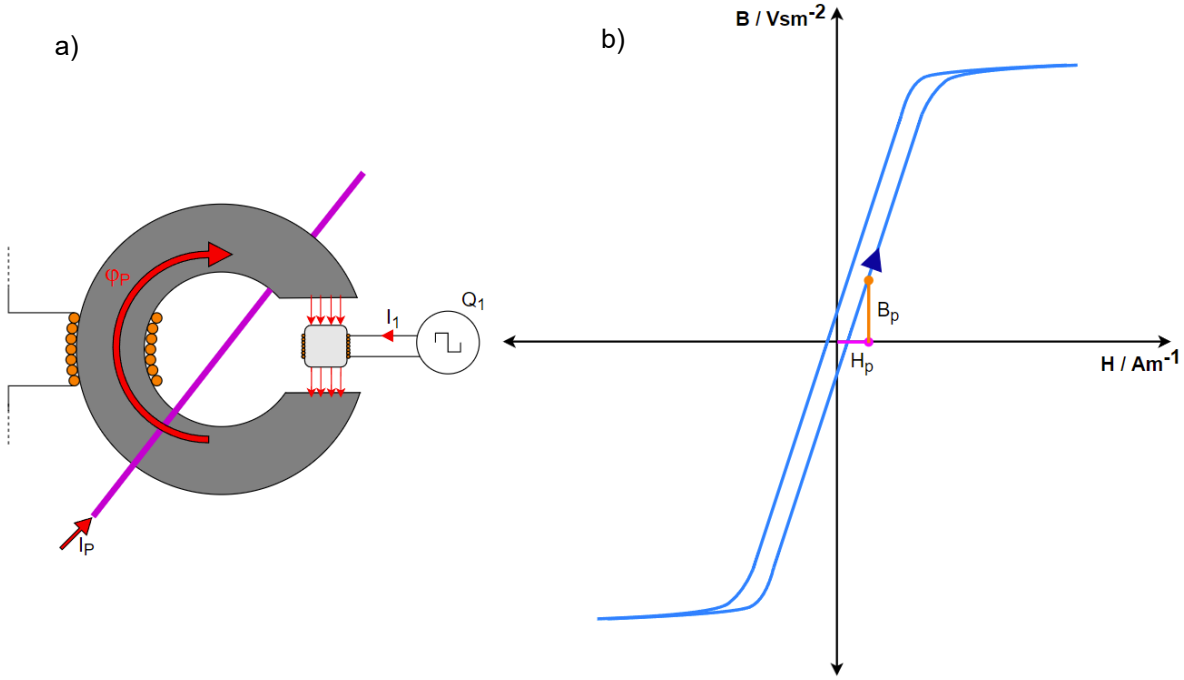


Figure 29: Abstracted structure of the fluxgate current sensor with a current-carrying conductor passing through it, source: self-created.

[25] Cf. Berger/Wolf/Rieder (2018) p. 132.

Figure 30 shows the hysteresis loop shifted along the H-axis.

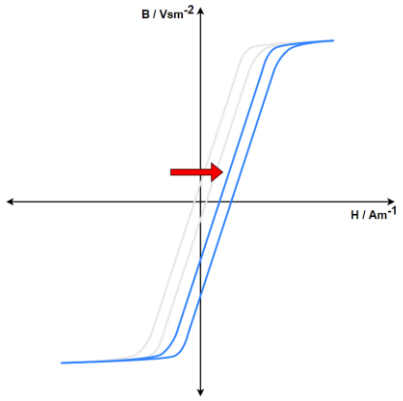


Figure 30: The hysteresis graph which was shifted along the H-axis due to the additional magnetic field strength HP, source: inspired by Berger/Wolf/Rieder (2018), p. 132.

Since the time until the fluxgate probe reaches saturation and the coil current exceeds the threshold value is greater in one direction than in the other, the output voltage of the oscillator is pulse width modulated as a function of a field *H*. The duty cycle of the output signal is very sensitive and is used for zero field detection in the air gap of the core. By energising the compensation winding, the magnetic flux in the iron core, and therefore also the magnetic field strength H_P in the air gap, is regulated to zero. The fluxgate probe is thus returned to a symmetrical operating point.[26]

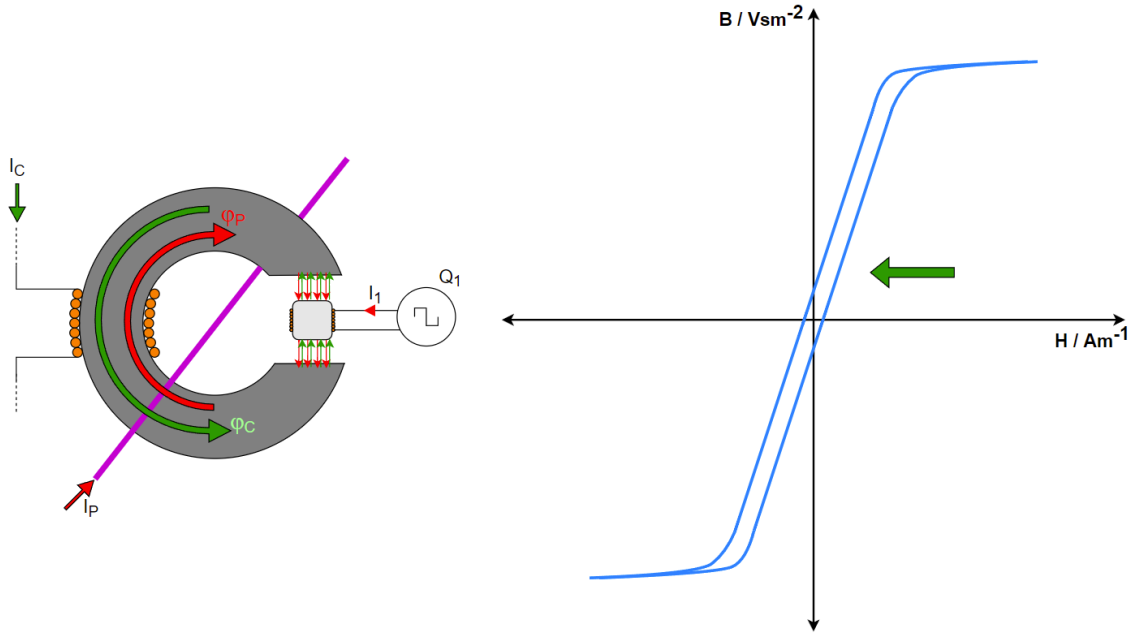


Figure 31: Abstracted structure of the fluxgate current sensor with a current-carrying conductor, and reverse current via the compensating coil Source: self-created.

Figure 31 shows how the magnetic flux φ_C generated by the control current I_C affects the total flux through the iron core and the iron core of the fluxgate probe. φ_C must be of the same magnitude as the flux φ_P but

[26] Cf. Berger/Wolf/Rieder (2018) p. 132.

have the opposite effect. The regulating current also serves as a measuring current which provides information about the current I_P. The current can either be analysed directly or evaluated using a measuring resistor R_M. The measuring current can be analysed according to equation (4.3), for example.

$$U_{out} = R_M \cdot I_C \tag{4.3}$$

U_{out}/V Output voltage

R_M/Ω Measuring-resistor

I_C/A Control current

6.3 Final measurement setup

Figure 32 and Figure 33 show the electrical layout diagram for measuring fuel cells and electrolysers using the cell monitor. The maximum configuration is shown, with consideration of the complete functionality.

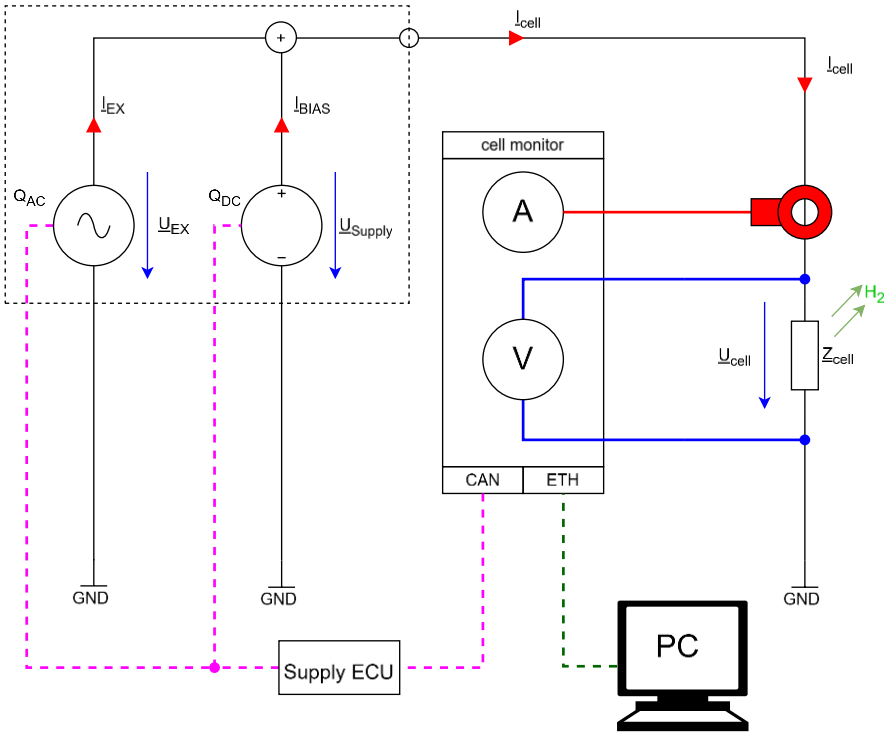


Figure 32: Final measurement setup for measuring an electrolysis stack or individual cell using four-wire voltage measurement and current measurement via fluxgate sensor, source: self-created.

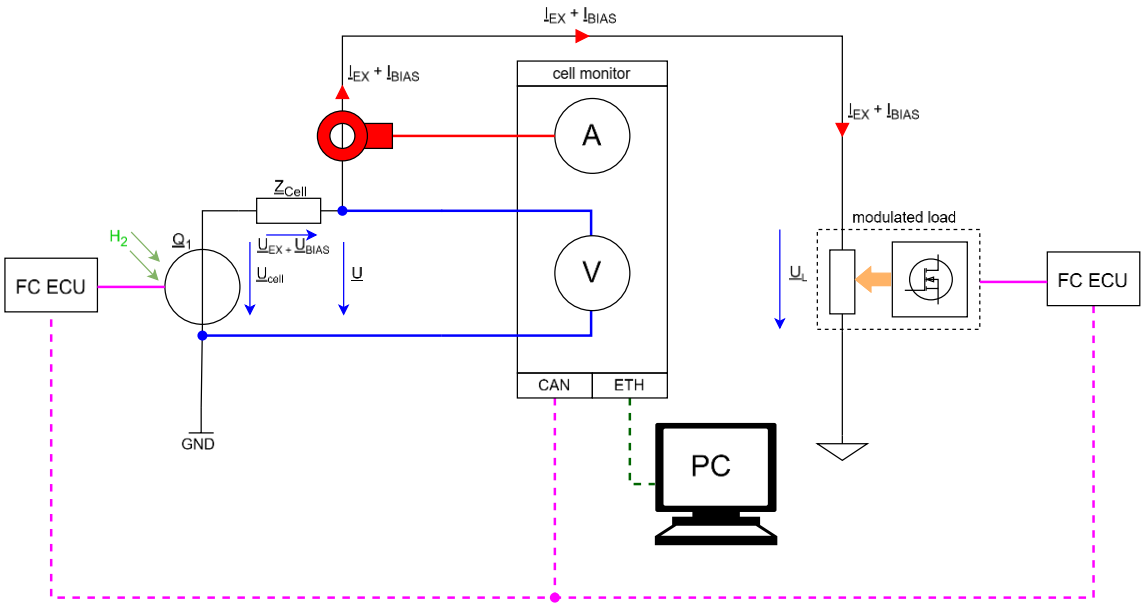


Figure 33: Final measurement setup for measuring a fuel cell using four-wire voltage measurement and current measurement via fluxgate sensor, source: self-created.

7 IMPLEMENTATION

Based on the findings from the theoretical part, the following steps are taken: In the first step, all the required macro modules, Ethernet switch and SBC of the cell monitor are evaluated. The existing circuit diagram of the cell probe prototype is then analysed. Based on these results, the new circuit diagram with additional functions is created. Finally, the results of the circuit design are combined with the selected modules to create a concept for the cell monitor.

7.1 Conceptualisation of the cell monitor

The cell probe is a microcontroller-based electronic module. Therefore, the operating software, the so-called firmware, must be transferred to the microcontroller. This is done with a programming device. Additionally, some programming devices provide the function of hardware debugging. Such a programming device is to be installed permanently in the cell monitor. As a result, the ease of maintenance is increased.

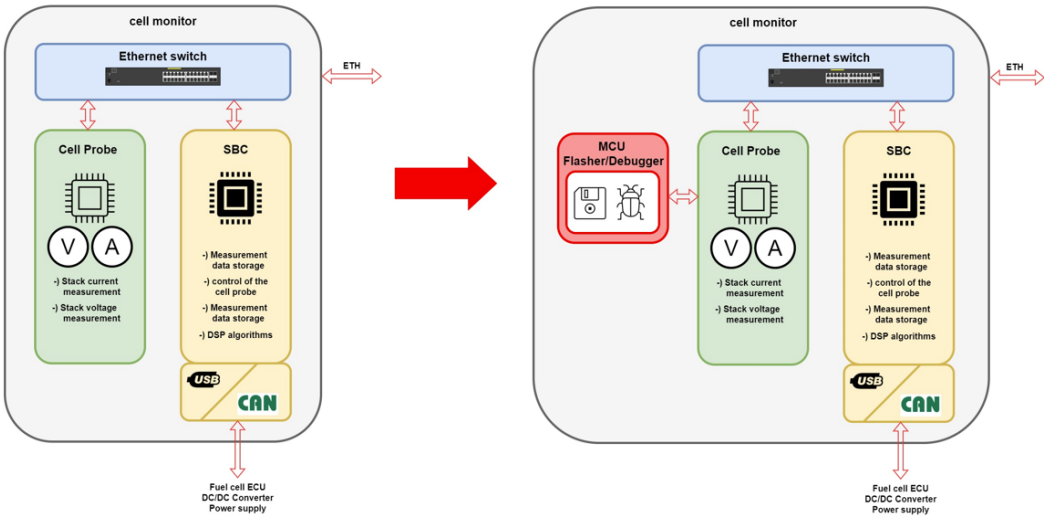


Figure 34: Extension of the cell monitor scheme by a microcontroller programming device, source: self-created.

7.1.1 Microcontroller programming unit

An STM32H747BIT6 microcontroller from the manufacturer ST-Microelectronics is used. This is a 32-bit ARM M7F microcontroller. This type was already used for the prototype of the cell probe. In order to be able to adapt the existing firmware as a basis for the new cell probe, the same type is used.

For this purpose, a suitable programming device was evaluated and chosen on the ST-Microelectronics homepage. The most suitable device for the purpose is the STLINK-V3MINE programmer. This supports the STM32H747BIT6 and offers SWD and JTAG as debugging standard.[27] The STLINK-V3MINE probe is designed as a PCB module and is therefore well suited for use in the cell monitor in terms of size. The programmer is supplied with the USB power supply of the programming device, e.g. a notebook.

[27] Cf. STMicroelectronics (2021), Online-Source [17.12.2023] p. 1.

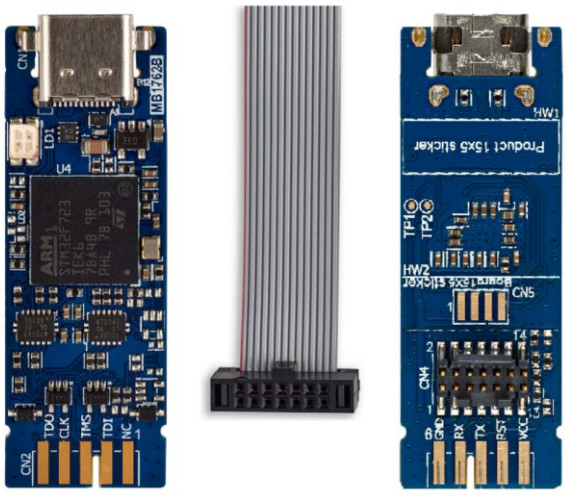


Figure 35:Top, bottom view of the STLINK-V3MINE probe including cable for programming the STM32H743ZI, source: STMicroelectronic (2024), Online-Source [1.1.2024], p. 1.

For use in the cell monitor, the probe is to be installed in a housing in order to provide mechanical protection for the STLINK-V3MINE and to enable the programmer to be mounted inside the housing of the cell monitor.

In addition to the STLINK-V3MINE, a USB hub is incorporated. This allows the microcontroller of the cell probe to be programmed and debugged both through the integrated SBC and via a dedicated USB interface on the housing. This enhancement is aimed at improving the usability of the cell monitor.

Figure 36: The ST4300MINU3B 1 to 3 USB hub from StarTech, source: StarTech (n.d.), Online-Source [1.1.2024] p. 1.

7.1.2 Ethernet switch

In the realization of a comprehensive system, the deployment of an Ethernet switch is envisaged. This is situated within the housing of the cell monitor. The minimum connectivity requirements necessitate three connections via RJ45 for Ethernet transmission, facilitating communication between the SBC, the cell probe, and the optional host computer. Furthermore, a dedicated connection for the power supply of the switch must be provisioned.[28]

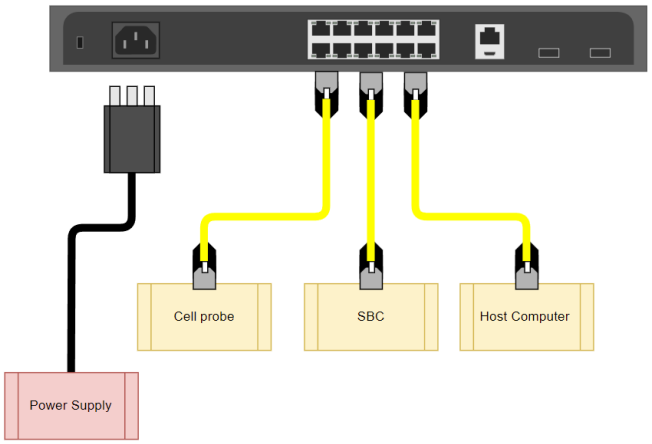


Figure 37: Illustration of the necessary Ethernet connections of the internal modules of the cell monitor, source: self-created.

The following type of Ethernet switch is used. The NITE-RS5-2100 from the manufacturer TERZ. In terms of Ethernet connectivity, the NITE-RS5-2100 fulfils the required three connections and has two additional ones. The NITE-RS5-2100 enables a data transfer rate of up to 1000 Mbit/s and requires a power supply of 9 to 36 VDC and a maximum current consumption of 130 mA. The device has dimensions of 103 mm x 77,4 mm x 22,5 mm. The operating temperature is between -40 C° and 70 C°.[29] A screw terminal serves as the power supply connection.

Figure 38:The NITE-RS5-2100 from the manufacturer TERZ, source: From an online shop Automation24 GmbH (n.d.), Online-Source [30.12.2023].

[28] Translation assistance by ChatGPT.

[29] Cf. TERZ Industrial Electronics GmbH (2021), Online-Source [27.12.2023] p. 2.

7.1.3 Single Board Computer

A Raspberry Pi 3 Model B+ served as the SBC in the predecessor of the cell monitoring system. Given the current unavailability of this particular SBC, an alternative SBC is to be employed. The chosen alternative should, at a minimum, adhere to the specifications of the Raspberry Pi 3 Model B+.

Figure 39: Top view of the Raspberry Pi 3 Model B+, source: Raspberry Pi Ltd 2023, Online-Quelle [30.12.2023] p. 2.

A single board computer from the manufacturer AAEON is used. The specifications of the Raspberry Pi 3 Model B+ are compared with those of the UP-APL03X7F-A10-0464 from AAEON in order to ensure compliance with the minimum requirements on the one hand and to illustrate the extended possibilities of the UP-APL03X7F-A10-0464 on the other.

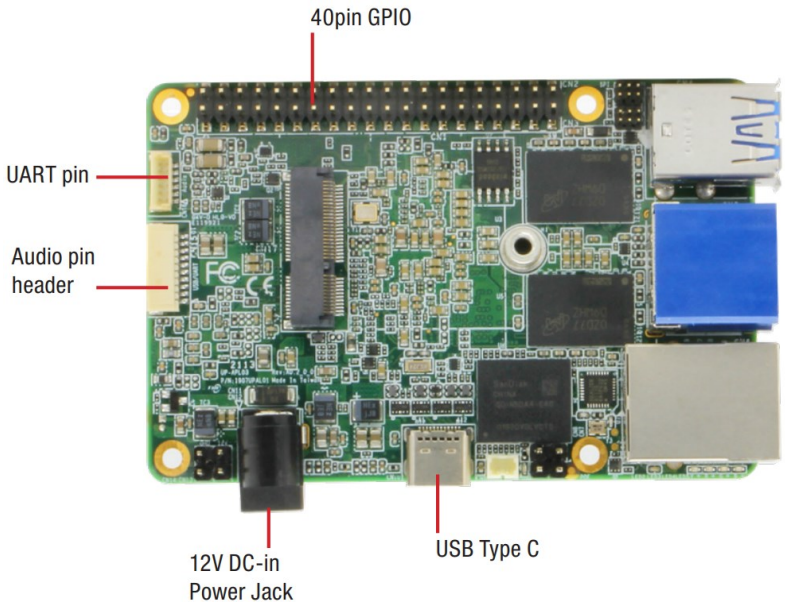


Figure 40: Top view of the UP-APL03X7F-A10-0464, source: AAEON Technology Inc. (2023), Online-Source [30.12.2023] p. 1.

All technical parameters were extracted from the datasheet for the Raspberry Pi 3 Model B+[30] and similarly for the UP-APL03X7F-A10-0464[31]. The tabular representation and alignment of these data are presented in Table 2. Only parameters and built-in functionalities of the SBCs deemed pertinent to utilization in the cell monitor have been taken into consideration.

Specification	Raspberry Pi 3 Model B+	UP-APL03X7F-A10-0464
CPU	quad-core Cortex-A54 64-bit SoC at 1,4 GHz	Intel Atom® x7-E390 quad-core at 2,00 GHz[32]
GPU	built in SoC VideoCore IV 32-bit at 400 MHz[33]	built in SoC Intel® HD Graphics
RAM Memory	1 GB	4 GB
Onboard ROM Memory	none	64 GB
I/O	GPIO Header	GPIO Header
USB	4 x USB 2.0	2 x USB 2.0 3 x USB 3.2 Gen 1 (A) 1 x USB 3.2 Gen 1 (C)
Ethernet	1 x 300 Mbps	1 x 1000 Mbps
RTC	no	yes
OS Support	yes	yes
Power Consumption	12,5 W (max) by 5 VDC	25 W (max) by 12 VDC
Operating Temperature	0 – 50 C°	0 – 60 C°
MTBF	not specified	538.629 h
Dimension	85 mm x 56 mm	85 mm x 56 mm

Table 2: Benchmarking between Raspberry Pi Foundation's SBC platforms and those from AAEON, source: self-created.

The UP-APL03X7F-A10-0464 fulfils all requirements of the Pi 3 B+ and surpasses the Pi 3 B+ in most categories. Consequently, the UP-APL03X7F-A10-0464 serves as a suitable replacement, expanding the operational capabilities and performance spectrum of the new cell monitor.

[30] Cf. Raspberry Pi Ltd (2023), Online-Source [30.12.2023] p. 1 – 4.

[31] Cf. AAEON Technology Inc. (2023), Online-Source [30.12.2023] p. 1 – 2.

[32] Cf. Intel technologies (n.d.), Online-Source [1.1.2024].

[33] Cf. Raspberry Pi Ltd (2023), Online-Source [1.1.2024].

The sole drawback pertains to the operating temperature range, as the Requirements (5.2 page 20) mandate a temperature range of -20 to 60 °C. In the subsequent development stemming from this thesis, a thermal analysis must be implemented to ascertain the extent to which a thermal management system is required. It should be examined whether the operational management of the cell monitor can mitigate this vulnerability.

7.1.4 Optional hard disc

For exhibition purposes, an optional hard drive can be integrated into the cell monitor, enabling data logging functionality. One of the USB 3.2 interfaces of the SBC can be utilized for both data connection and power supply. The recording duration, contingent upon the storage capacity of the hard drive and the data format of the observed parameters, can be derived through the following correlation.

$$t_{rec} = \frac{S_{HD}}{D_{para} \cdot f_{sample}} \quad (5.1)$$

$$D_{para} = \frac{\sum_{i=m}^{n} Data_i}{8\,{}^{Bit}/_{Byte}} \quad (5.2)$$

t_{rec}/s	Recording duration
S_{HD}/Byte	Hard disc storage capacity
D_{para}/Byte	Data storage requirements
f_{sample}/s^{-1}	Sampling frequency
$Data_i$/Bits	Digitised measured values

A potential model of an external hard drive has been researched, although its operating temperature range does not align with the specified range. (see Figure 41)

SKU	INSSD480GPORT3.0
EAN	5055288436138

	Width (mm)	**Depth (mm)**	**Height (mm)**	**Weight (g)**
Product	49	9	80	41
Packaging	119	21	132	105

Capacity (GB)	480
Read speed (MB per second)	400MB/s
Write speed (MB per second)	370MB/s

USB version	3.2 Gen 1 (3.1 Gen 1)
Protection features	Shock resistant
Device interface	USB Type-A
Product colour	Black
Operating temperature (T-T) (degrees Celcius)	0 - 70
Storage temperature (T-T) (degrees Celcius)	-25 - 85
Quick start guide (Y/N)	Y
Cables included	USB Type-A
Certification	UKCA

Figure 41: Specification of the INSSD480GPORT3.0 from Integral Memory plc. source: Figure adopted from Integral Memory plc. (n.d.), Online-Source [1.1.2024] p. 1.

Nevertheless, a thermal analysis, analogous to the SBC, reveals the measurement scenarios in which this type can be employed. Alternatively, a hard drive suitable for lower temperature ranges may be considered.

Figure 42: Potential hard drive for cell monitors data logging, source: Integral Memory plc. (n.d.), Online-Source [1.1.2024].

The INSSD480GPORT3.0 provides a storage capacity of 480 GB. Therefore, with this external hard drive, an example recording duration could be achieved as follows.

Given that a cell voltage, the recorded total current, and the corresponding timestamp are each captured as a 32-bit number, the result for D_{para} is as follows:

$$D_{para} = \frac{Data_{voltage} + Data_{current} + Data_{timestamp}}{8\,{Bit}/{Byte}}$$

$$D_{para} = \frac{32\ \text{Bit} + 32\ \text{Bit} + 32\ \text{Bit}}{8\,{\text{Bit}}/{\text{Byte}}} = 12\ \text{Byte}$$

Hence, the recording duration, assuming a sampling frequency of 25 kHz, is as follows:

$$t_{rec} = \frac{480 \cdot 10^9 \text{Byte}}{12\ \text{Byte} \cdot 25 \cdot 10^3 \text{s}^{-1}} = \frac{1{,}6 \cdot 10^6 \text{s}}{3600\,\frac{\text{s}}{\text{h}}} = 444{,}4\ \text{h}$$

7.1.5 USB to CAN-Converter

A USB to CAN converter of the type “simplyCAN” by Ixxat is employed.

The device operates without requiring an additional driver installation and can be operated through the provided API interface.[34]

Figure 43: Ixxat's USB to CAN converter, source: HMS Industrial Networks (n.d.), Online-Source [1.1.2023].

[34] Cf. HMS Industrial Networks (2020), Online-Source [1.1.2024] p. 1.

7.2 Cell monitor housing concept

Considering the variable operating environments of the cell monitor, which may not always pose potential risks of liquid ingress, a conventional metal enclosure lacking specific liquid protection mechanisms is employed. An individually customized enclosure will be manufactured by industrial providers for the cell monitor. Below is an exemplary depiction of a metal enclosure for the cell monitor.

Figure 44: Example enclosures which can be customised by Schaeffer AG, source: Schaeffer AG (n.d.), Online-Source [1.4.2024].

To operate the cell monitor in environments requiring moisture protection according to IP54 standards, it is installed in an additional enclosure, with all cables routed through suitable cable glands. The cables are guided to the cell monitor within the supplementary enclosure using a cable gland system, as depicted in Figure 45.

Figure 45: Possible cable entry system from Weidmüller for use of the cell monitor in an IP54 environment, source: Weidmüller GmbH (n.d.), Online-Source [1.4.2024].

This results in the following advantages regarding connector specifications: On the one hand, connectors for all interfaces provided by the cell monitor can be implemented with standard connectors, which are both more cost-effective and offer a greater variety of connector types. However, a disadvantage is that the volume requirement of the cell monitor increases in an environment demanded by IP54.

7.3 Intermediate overview of the cell monitor

Figure 46 depicts the cell monitor with all integrated sub-components. The data connections between individual components are also illustrated, and the known voltage supply requirements for each sub-component are specified. The hard drive, USB to CAN converter, USB hub, and MCU Flasher/Debugger are interconnected via USB, with power supply ensured through the USB interface (Power over USB). An additional USB connection is implemented for programming the cell probe MCU, allowing programming via either the Single Board Computer (SBC) or an external programming device. The 40 GPIOs provided by the SBC are externally accessible via wire terminals. This facilitates the connection of additional control electronics such as PWM modules, relay boards, or transistor stages, enabling the cell monitor to assume additional control functionality for potential measurement, control, and regulation tasks within the overall test setup.[35]

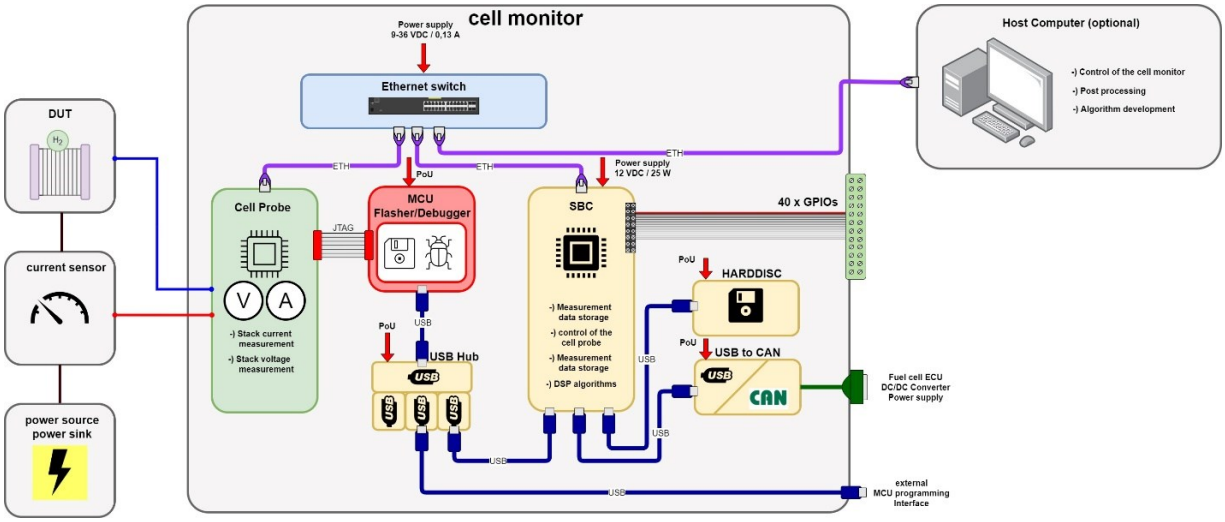


Figure 46: Schematic Structure of the Cell Monitor, including all sub-components and optional elements, data connections, and power supply requirements, source: self-created.

[35] Translation assistance by ChatGPT.

8 CELL PROBE

To gain understanding of the functionality of the current schematic diagram for the cell probe, it underwent analysis and was presented as a block diagram in section 8.1. The functionalities are categorized into distinct modules, each depicted by individual blocks. Building upon these insights, the new schematic diagram for the cell probe is designed, considering the following aspects:

- Availability of components
- Assessment of functionality
- Integration of new features
- Implementation of protective circuitry
- Adherence to specified requirements for measurement quality

The development process (8.2) of the new schematic diagram proceeds as follows: Each circuit block of the existing design undergoes examination to determine whether it can be adopted without modification, requires revisions, should be discarded, or necessitates the integration of entirely new circuitry. The outcome of this process is presented in this chapter, illustrating the revised schematic diagram of the cell probe.

8.1 Review of the prototype schematic

The first step involves examining the power supply concept of the current cell probe, followed by an analysis of its functionality. The original schematic diagram of the current version of the cell probe is located in the appendices.

8.1.1 Power supply concept

The power supply for the Cell Probe is initiated through a central connection point via a plug. In this process, the 24 VDC is divided into three branches. One branch generates the power supply for the sensors (Figure 47 path A). The sensor supply creates a +/-15 VDC power supply from the supplied 24 VDC, which is simultaneously galvanically isolated. This supply is used to power the Fluxgate current sensor. The galvanic isolation enhances the interference immunity of the circuitry. The current sensor V-supply is directly routed to the Fluxgate sensors via a connector.

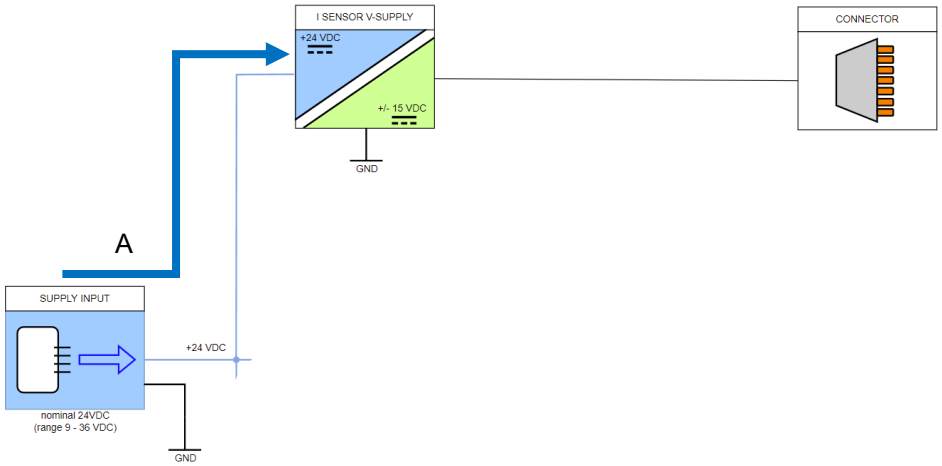


Figure 47: Partial representation of the voltage supply structure of the prototype Cell Probe with Fluxgate supply, source: self-created.

In Figure 48 B, the branch denoted as "Main Supply" is depicted. It also derives from the input voltage supply. In the initial stage, +/-15 VDC is generated without galvanic isolation. From these +/-15 VDC, 5 VDC, 3,3 VDC, and 3 VDC are respectively derived. These voltage levels supply the control electronics, such as the microcontroller in the current version of the Cell Probe. The calibration branch is also supplied by these branches.

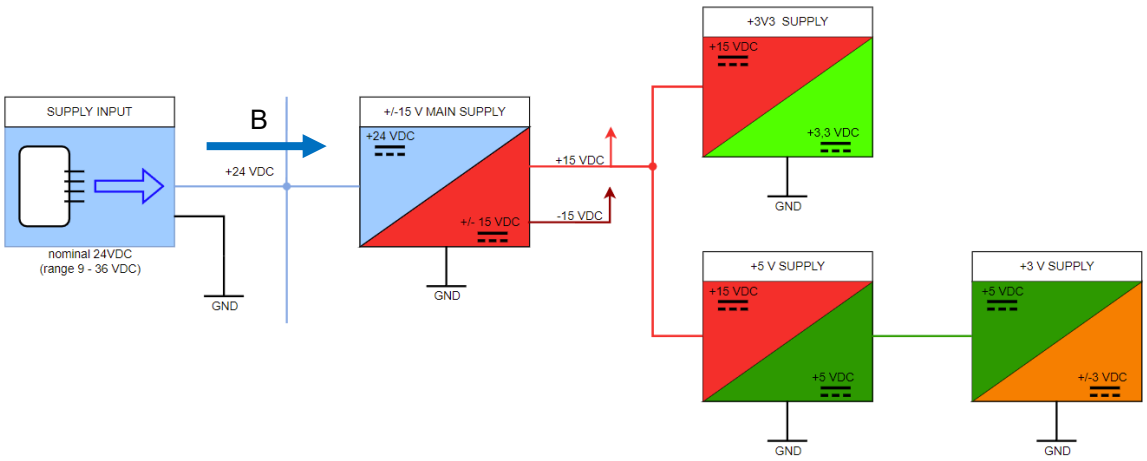


Figure 48: Segment of the power supply representing the general voltage supply, source: self-created.

The final branch (Figure 49) serves the power supply needs of the measurement electronics, including the ADCs and associated filters. From the 24 VDC input, a galvanically isolated 15 VDC supply is generated. From this 15 VDC voltage level, a +/-12 VDC, a 5 VDC, a 3,3 VDC, and finally a 3 VDC power supply are derived. The entire voltage supply tree is illustrated below Figure 49.

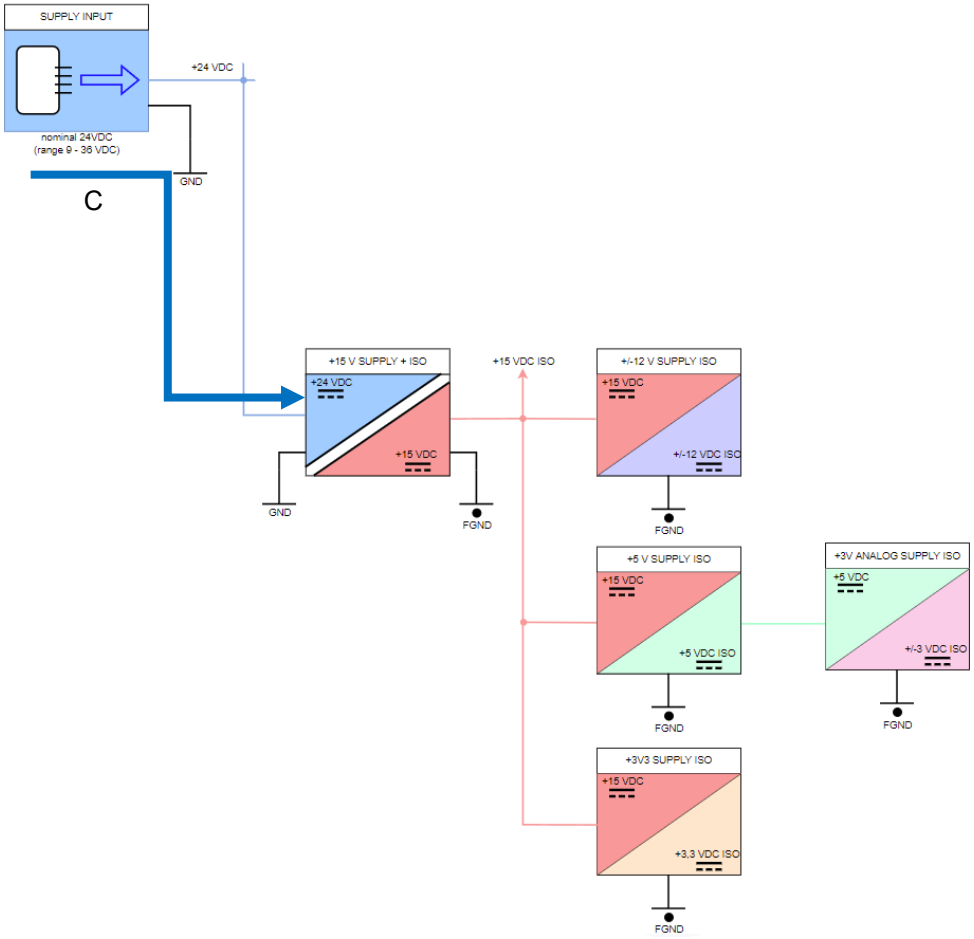


Figure 49: The galvanically isolated Branch C serves as the power supply for the measurement electronics, source: self-created.

Figure 50 The figure provides an overview of the power supply concept of the current version of the Cell Probe. It illustrates the various components and their interconnections.

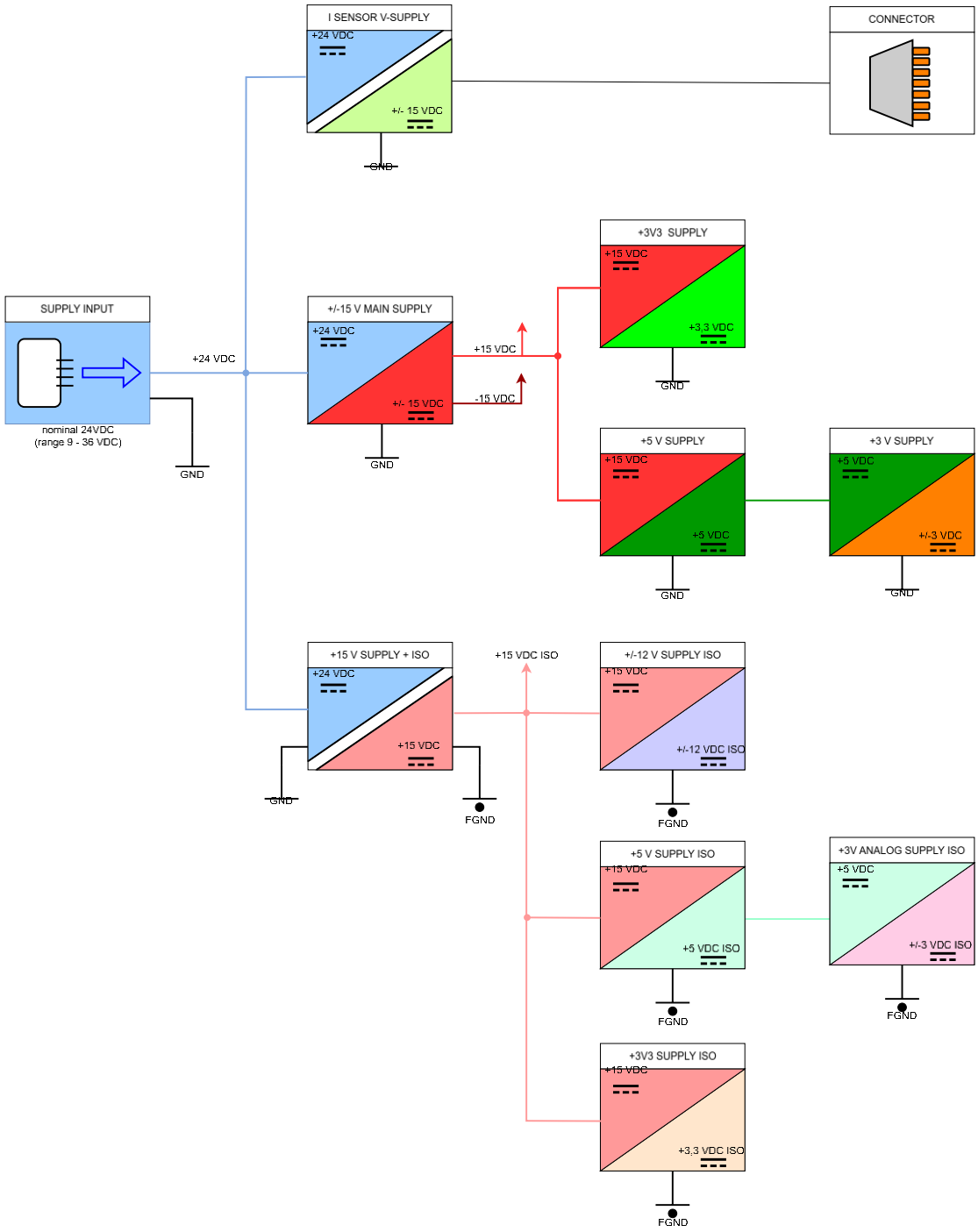


Figure 50: The overall topology of the voltage supply for the currently used cell probe, source: self-created.

8.1.2 Functional circuit parts

Figure 51 represents the entire functional schematic as a block diagram. The colours of individual blocks symbolize the respective connected power supplies, as detailed in Chapter 8.1.1 on page 43.

In Figure 51 a, the microcontroller unit is depicted. The microcontroller of type STM32H743ZI is integrated in the form of a development board, specifically the NUCLEO-H743Z12 board from STMicroelectronics. Through this microcontroller board, all circuit components of the current cell probe are controlled. Additionally, the NUCLEO-H743Z12 features an Ethernet interface through which the cell probe can communicate with other modules and devices. Furthermore, CAN communication is facilitated through a UART interface and a UART-to-CAN converter IC, as shown in Figure 51 b.

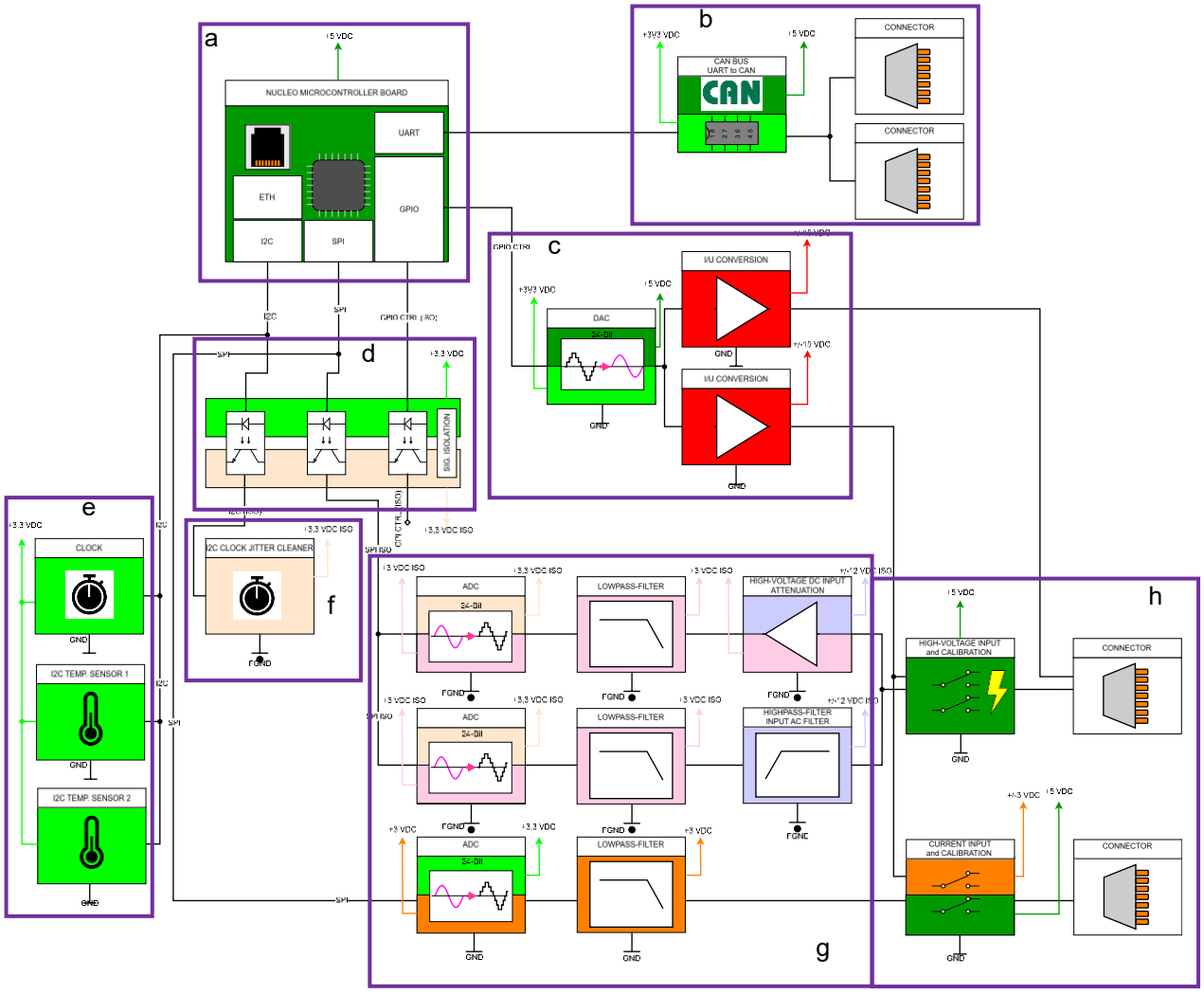


Figure 51: Overview of all integrated circuit components in the functional circuit, source: self-created.

Connected to a general-Purpose input/output (GPIO) port is sub-circuit c, which includes a digital-to-analog converter (DAC) and additional filters and circuit components for its operation. The DAC generates signals used to calibrate the measurement channels of the cell probe. The generated DAC signal is converted from a current to a voltage signal through filters and additional analog circuit components. The processed signals are directed both directly to connectors and, via two additional

blocks, to the High-Voltage Input and Current-Input (Figure 51 h). The High-Voltage Input and Current-Input blocks serve as switches between measurement and calibration signals. Within the Current-Input block, there is an analog circuit that converts the measurement signal from the current sensor into a voltage signal.

The current and voltage measurement signals, routed through the High-Voltage Input and Current-Input blocks, are each subjected to an ADC (Figure 51 h). The voltage measurement signal is separated into a High-Voltage Direct Current signal and an Alternating Current signal. The High-Voltage DC signal is attenuated to a lower voltage level by the High-Voltage DC Input attenuation block, with a maximum of 1000 VDC applicable at the input. The DC Input attenuation reduces the voltage to one four-hundredth. The AC component of the voltage measurement signal undergoes filtering through a 3rd-Order Butterworth high-pass filter. Both voltage measurement signals, along with the previously converted current measurement signal, pass through a 3rd-Order Butterworth Lowpass filter before being processed by an ADC.

The digital values generated by the ADC for the measurement signals are transmitted via the SPI bus to an interface IC, which implements galvanic isolation between the measurement circuit and the data-processing microcontroller. The data path extends from circuit block g through d to circuit block a. The Jitter Cleaner, connected via I^2C, generates the sampling frequency for the ADC, processing both the direct current measurement signal and the alternating current measurement signal, while simultaneously providing a clean clock signal.

Within circuit block e, another clock generator, connected via I^2C, is situated. The Clock block, among other functions, dictates the sampling frequency for the ADC that digitizes the current measurement signal. The digitized measurement values are also processed by the microcontroller through the SPI bus, which, in this case, is not galvanically isolated. The two temperature sensors, I^2C TEMP Sensor 1 and Sensor 2, measure the temperature inside the housing where the cell probe is installed. Figure 52 depicts the structure of the current version of the cell probe board with an open housing.

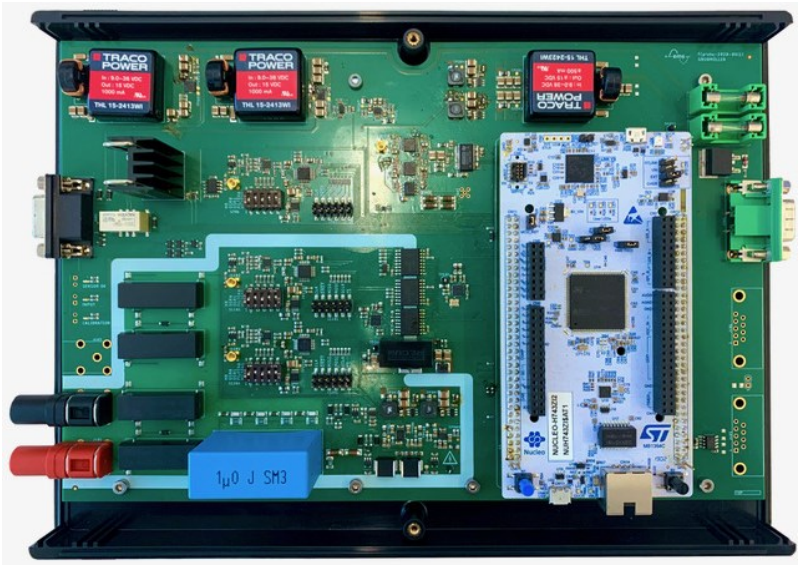


Figure 52: Circuit board of the current version of the cell probe installed in the housing, source: self-created.

8.2 Circuit design

At this stage, the new schematic diagram for the cell probe is being developed using kiCAD as the Electronic Design Automation (EDA) software. The hierarchical schematic design method is employed, where all circuit components are organized into hierarchical blocks containing their respective functionalities. This approach offers several advantages: it enhances clarity by providing a clearer overview, facilitates easier interchangeability of circuit blocks, and allows for the addition of new blocks for future developments. The old as well as the new circuit diagrams have been attached in the appendices.

8.3 Power supply

In the first step, the setup of the power supply for the new cell probe board is implemented. The supply voltage is introduced via the block 1 “DEVICE POWER SUPPLY INPUT” (Figure 53). It is necessary for the employed power supply to have an output power of min. 150 W to ensure a stable supply. The introduced supply is distributed to blocks 2, 4, and 6. Block 2 represents the equipment supply for the cell monitor, with the generated 12 V provided via PCB terminals in block 3 for the connection of the SBC, etc. block 4 supplies the electronics of the cell probe itself, while block 5 provides supply for the voltage measurement path. As voltages up to 1000 V can be measured, block 5 has been electrically isolated from the other power supply blocks. Behind block 6 is the voltage supply unit, which provides supply for the fluxgate current sensors.

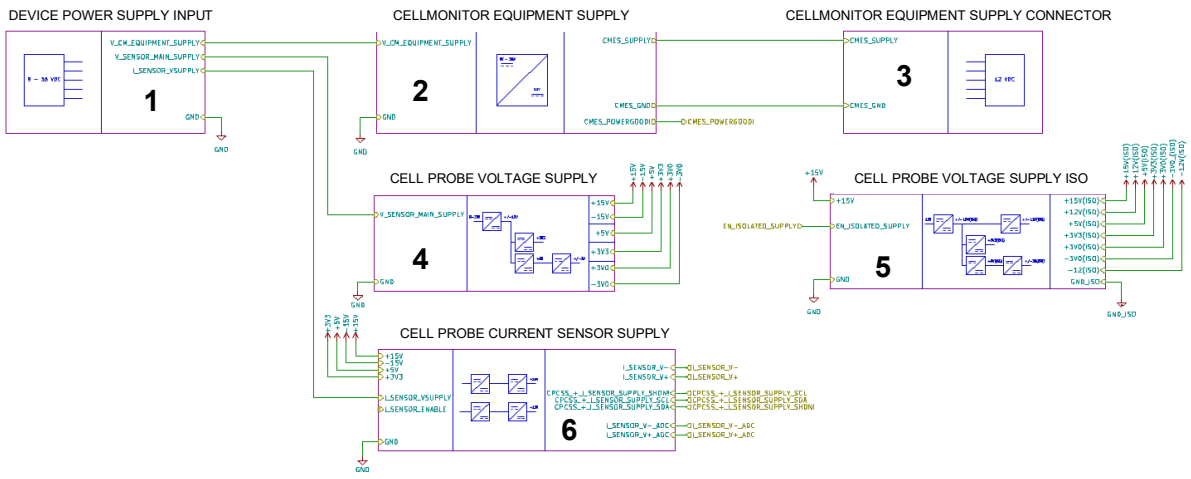


Figure 53: Structure of the cell probe power supply concept including the equipment supply, source: self-created.

8.3.1 Device power supply input

The input voltage supply is divided into three supply branches. One branch is designated for the equipment, which is placed before the branches for the sensor supplies. The sensor voltage supplies are protected by fuses. Transistor Q11 in combination with D12 and R59 provides reverse polarity protection. For the input connector, a through-terminal terminal block is employed, which is directly mounted within the housing. On the output side, wires are connected and soldered directly to pads. The terminal blocks offer the advantage of eliminating the need for a connector to establish the power supply of the cell monitor. (See Figure 54)

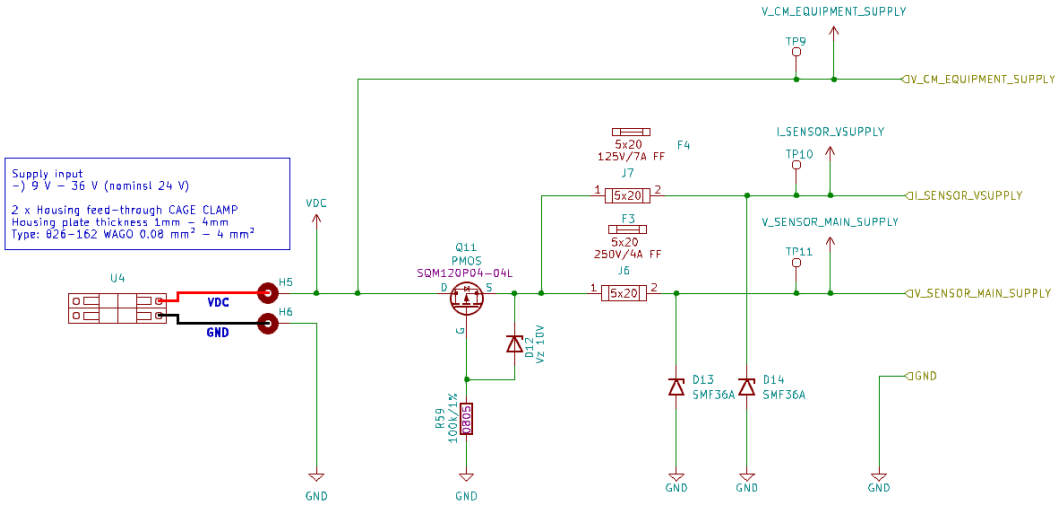


Figure 54: Circuit of the hierarchical block device power supply input, source: self-created.

8.4 Cell monitor equipment supply

In order to operate the Cell Monitor, not only a power supply for the cell probe is required, but also a voltage supply for the SBC and it's connected components, as well as for the Ethernet switch. The power supply for both the SBC and the Ethernet switch was implemented in the prototype using additional external voltage supplies. However, by incorporating an additional voltage regulator, the need for external power supplies becomes obsolete, leading to cost savings in component expenses and simplification of wiring efforts.

The power supply for the cell monitoring equipment consists of two circuit units. One of these is a protection circuit that detects both over and under voltage and includes functions for overcurrent and reverse current protection. This protection circuit is implemented using the LTC4368. To maintain the input voltage range specified at 9-36 V, a buck-boost voltage regulator is implemented for the power supply. The voltage regulation is achieved through the LT8390A IC, which is a synchronous four-switch buck-boost voltage regulator.

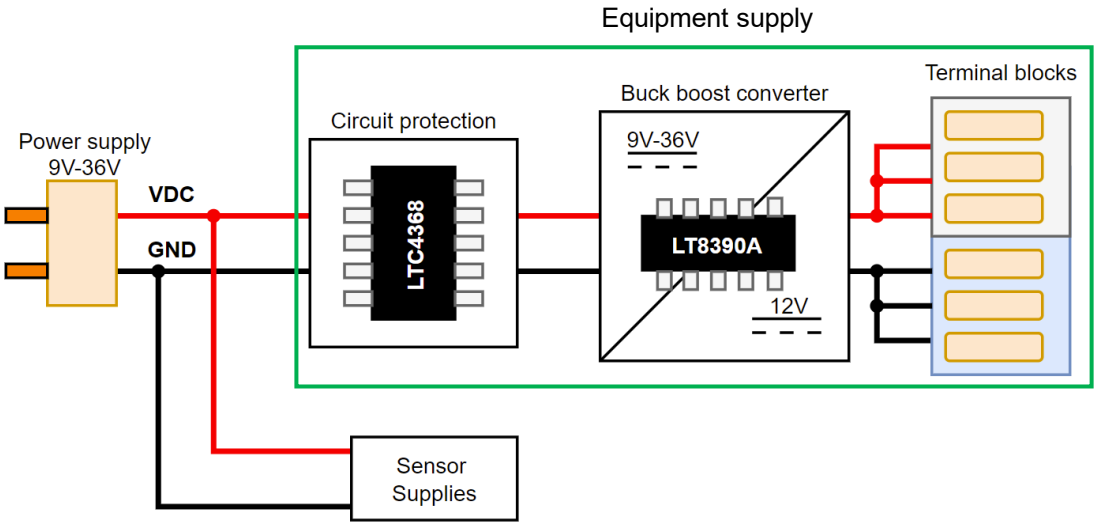


Figure 55: Schematic layout of the cell monitor equipment supply, source: self-created.

The modules of the Cell Monitor show a power consumption of approximately 27 W in total, equivalent to a load current of around 2.25 A. Both the SBC and the Ethernet switch operate at 12 VDC, meeting the basic requirement for the buck-boost converter's specifications. Figure 56 illustrates an exemplary application of the LT8390A, serving as the foundation for the implementation process. The circuit diagram in Figure 56 indicates that a current of 4 A can be delivered at the output. This configuration is kept providing sufficient power reserves and ensure a safe operation of the SBC and Ethernet switch.

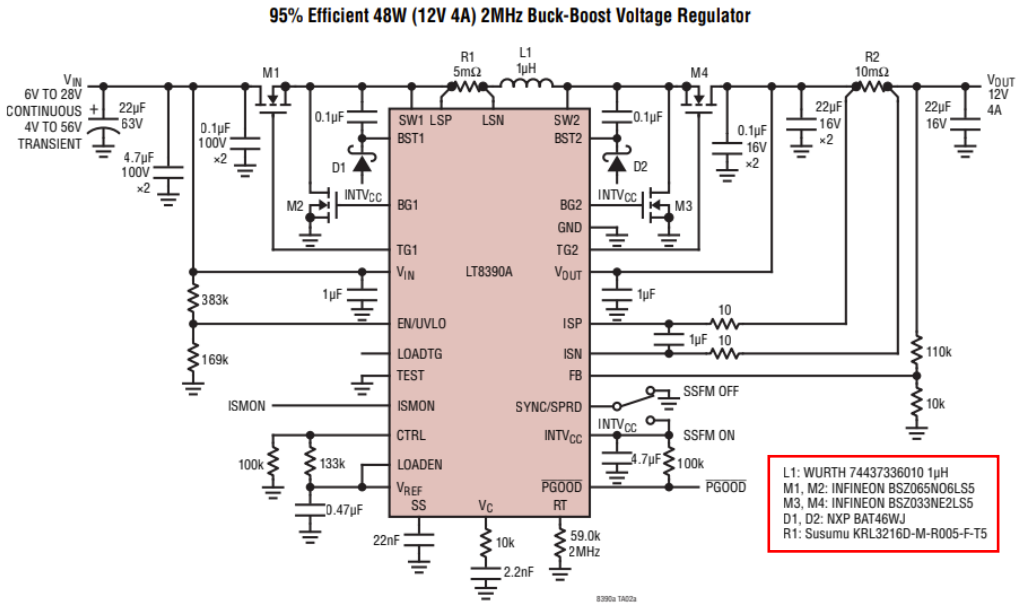


Figure 56: Example circuit of the LT8390A,
source: adopted ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 28.

Since the specified input voltage range of 9 V to 36 V does not match the input voltage range of the example circuit shown in Figure 56, it is necessary to assess the suitability of the components used in the

example circuit for the specified operating conditions. To achieve this, a simulation model[36] of the example circuit will be adapted to match the required input voltage range. Using this model, the critical components such L1 (inductance), Q1-Q4 (transistors), C_{in} (input capacitors), and C_{out} (output capacitors) will be validated.

To accomplish this, the following steps are implemented:

- **Adjustment of the simulation model:** Initially, the supply voltage is set to the required range of 9 V to 36 V. This involves evaluating the behaviour of L1 and transistors Q1-Q4, as well as assessing the output voltage and current.

- **Adjustments and Re-Simulation:** In the next step, any necessary adjustments are made to the transistors and the inductor L1 in the circuit. These changes are validated through a new simulation to ensure they meet the required specifications.

- **Input capacity design:** Subsequently, the input and output capacities are examined and revised if needed. This is crucial to ensure a stable and reliable power supply, and to identify and resolve potential issues.

- **Design of the LTC4368:** The permissible voltage hysteresis and all other functionalities are implemented.

- **Implementation in the Circuit Diagram:** Finally, the validated adjustments and specifications are implemented in the circuit diagram.

[36] Cf. ANALOG DEVICES, INC (n.d.), Online-Source [8.1.2024].

8.4.1 Adjustments of the Simulation Model

The switching frequency of the LT8390A is set by an internal oscillator. When the SYNC/SPRD pin is grounded, the switching frequency is determined by an external resistor connected to the RT pin to ground. The values of the RT resistors dictate the switching frequency.[37]

Figure 57 illustrates resistor values for common switching frequencies.

f_{OSC} (MHz)	R_T (k)
0.6	267
0.8	191
1.0	147
1.2	118
1.4	97.6
1.6	82.5
1.8	66.5
2.0	59.0

Figure 57: Resistor values in kΩ for setting switching frequencies,
source: ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 19.

To operate the voltage regulator at a switching frequency of 2 MHz, a resistor value of 59 kΩ is provided for the resistor connected to the RT pin. Opting for a high switching frequency reduces the required inductance of the coil, thereby affecting its size. Additionally, any potential disturbances from the switching regulator lie well above the specified 25 kHz of the signals being measured and can thus be filtered out.

The simulation will be implemented as a transient analysis, which will simulate the circuit at 9 V, 24 V, 24 V, and 36 V. Here, 9 V and 36 V represent the upper and lower limits for the allowable power supply voltage, while 12 V and 24 V are typical values for external power supplies used to supply power to the entire cell monitor system. The value of R_{LOAD} of 3 Ω sets the output current to 4 A. The load R_{LOAD} is active from the start of the simulation because this condition also occurs in the real applications. Additionally, the inductor model of 74437336010 was chosen according to the specification of the example circuit in Figure 55. The capacitors C2 and C5, representing C_{IN}, were removed to determine the raw input current of the LT8390A in the simulation. Figure 58 illustrates the adaptation process.[38]

[37] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 19.

[38] Translation assistance by ChatGPT.

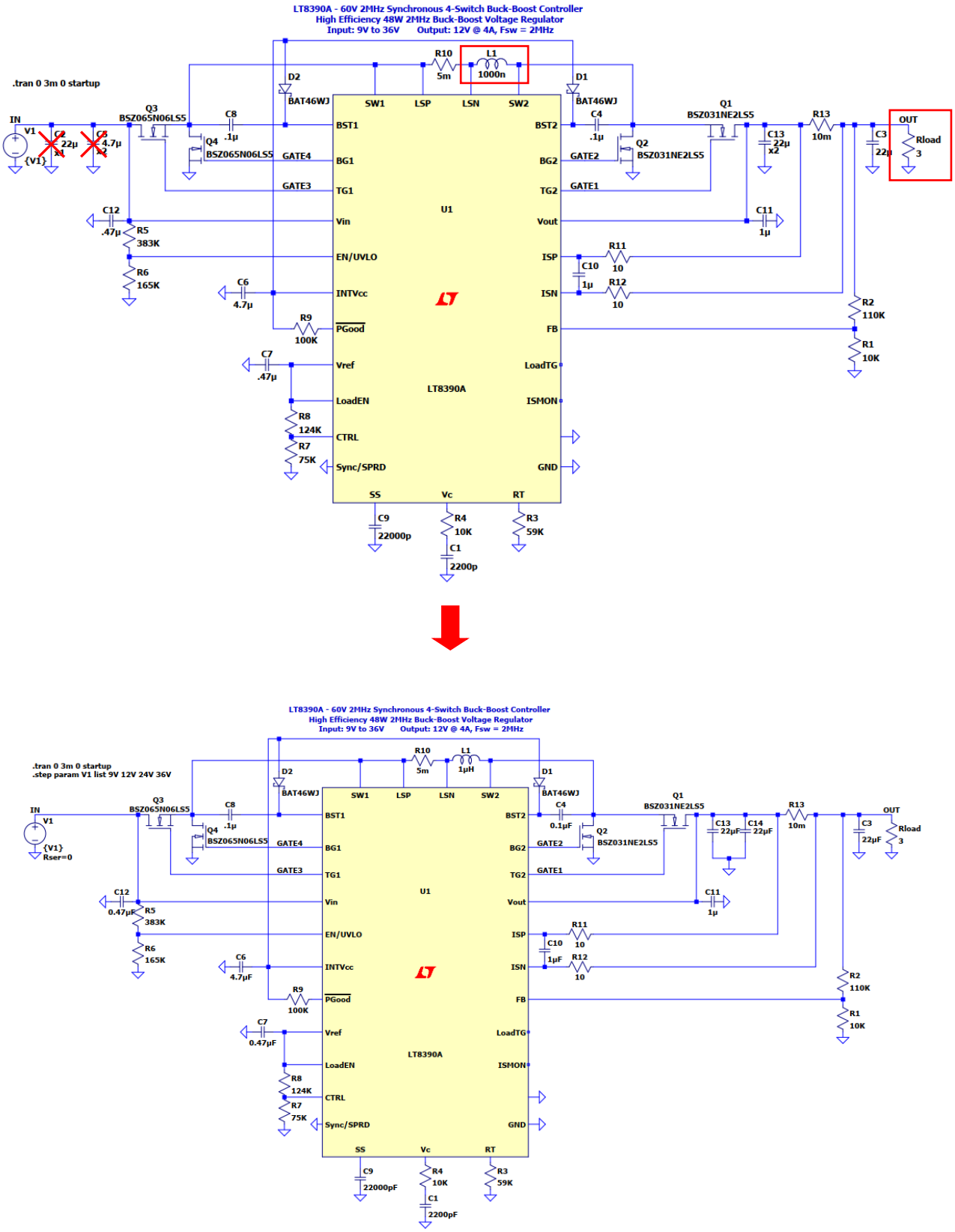


Figure 58: Customized simulation model of the LT8390A example circuit, source: self-created.

8.4.1.1 Analysis of inductor performance

The current $I_{(L1)}$ was measured across the inductor L1. It was observed that the regulator reaches its steady state after approximately 1.6 ms at an input volatge of 9 V. During the transient phase, the current in the inductor subject significantly changes. With an input voltage V_{IN} of 9 V, the LT8390A operates in the boost region, where the highest inductor current occurs (marking A in Figure 59 right). This point is further examined to avoid inductor saturation. Due to the extended simulation duration, the saturation of the inductor was not considered during the simulation. Therefore, it is necessary to assess saturation using parameters from the datasheet. This involves comparing the maximum current observed in the simulation with the specified saturation current provided in the datasheet.

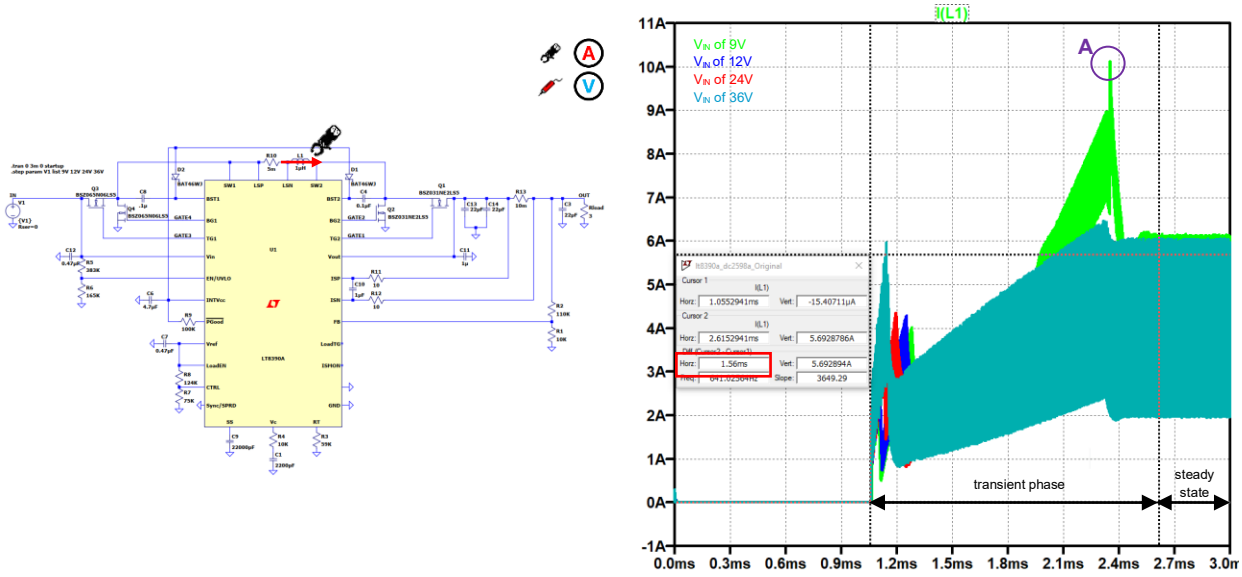


Figure 59: Left: Current measurement through L_1, right: Simulation results for the coil current through L1 for voltages of 9 V, 12 V, 24 V, and 36 V, source: both self-created.

According to Figure 60 (left), the maximum inductor current I_{L1} during the transient phase is approximately 10.2 A. In steady-state conditions, with a V_{IN} voltage of 36 V, the worst-case peak-to-peak ripple current ΔI_L is approximately 4 A (Figure 60 right), with an average current I_{AVG} of 4 A.

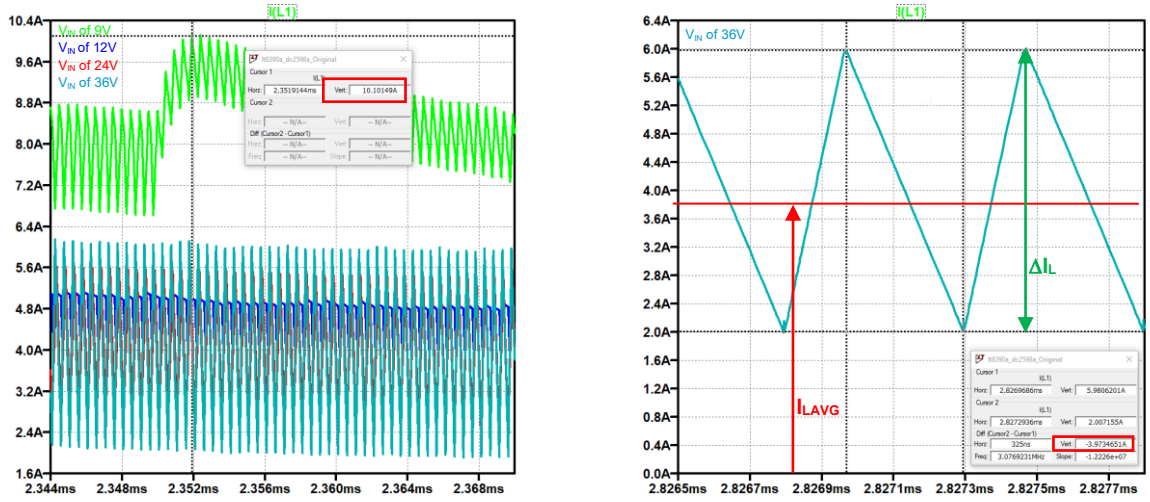


Figure 60: Left: Maximum current during over the time of the transient phase at an input voltage Vin of 9 V. Right: Capture of the maximum peak-to-peak ripple current at an input voltage Vin of 36 V, source: both self-created.

To evaluate the relationship between average current and peak-to-peak ripple current, equation (8.1) is introduced. Therefore, an average-to-ripple current ratio ($\Delta I_{L\%}$) of 100 % is obtained under steady-state conditions.

$$\Delta I_{L\%} = \frac{\Delta I_L}{IL_{\mathrm{AVG}}} \cdot 100\% \qquad (8.1)$$

$\Delta I_{L\%}$ Ratio of average current to ripple

ΔIL /A Peak-to-peak current ripple

IL_{AVG}//A Average current

The analysis of Figure 61 leftside reveals that at an input voltage of 9 V, an average current I_{AVG} of approximately 5.5 A is achieved with an average-to-ripple current ratio of about 21.8 %. During the transient phase, the I_{AVG} momentarily reaches a value of approximately 9.6 A average current.

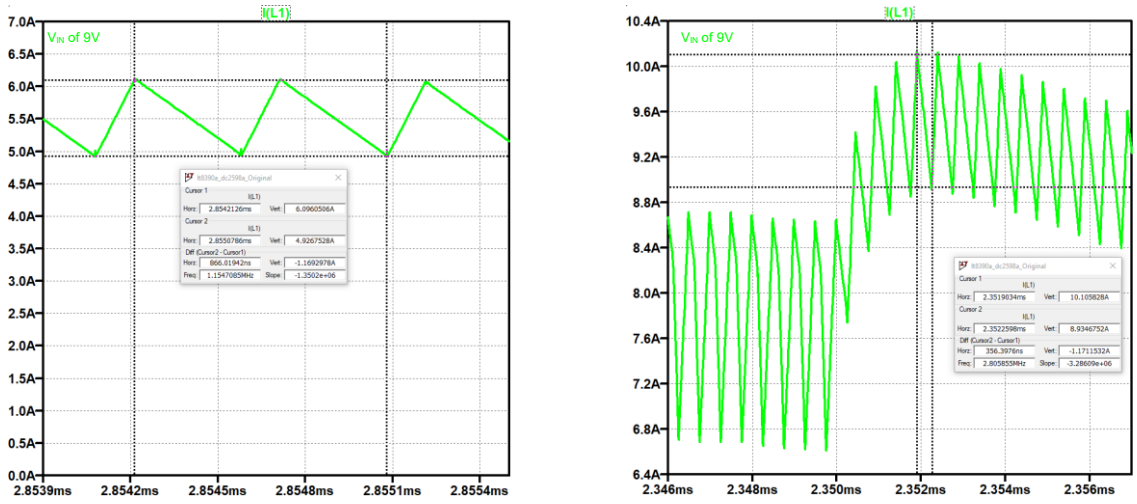


Figure 61: Left: Steady-state current over time with an input voltage of 9 V. right: Transient current curve over time at 9 V input voltage, source: both self-created.

Regarding the peak current of around 10.2 A with an I_{AVG} of 9.6 A during the transient phase at a 9 V power supply, the requirement for saturation-free operation of the inductor cannot be met. According to the electrical properties of the 74437336010 inductor, saturation-prone operation begins at 7.4 A with an average-to-ripple current ratio of less than 10 %. Therefore, an inductor with a higher permissible rated current must be used.

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 10 mA	1	µH	±20%
Rated Current	$I_{R,40K}$	ΔT = 40 K	7.3	A	max.
Performance Rated Current 1)	$I_{RP,40K}$	ΔT = 40 K	8.6	A	max.
Saturation Current @ 10%	$I_{SAT,10\%}$	|ΔL/L| < 10 %	7.4	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	14.2	A	typ.
DC Resistance	R_{DC}	@ 20 °C	13	mΩ	typ.
DC Resistance	R_{DC}	@ 20 °C	14	mΩ	max.
Self Resonant Frequency	f_{res}		60	MHz	typ.

1) refer to IEC 62024-2-2020

Figure 62: Permissible current carrying capacity of inductor 74437336010, source: adapted from Würth Elektronik eiSos GmbH & Co. KG 74437336010 (n.a.), Online-Source [25.2.2024] p. 1.

8.4.1.2 Analysis of Transistors

For the operation of the LT8390A, four transistors are required to act as switches. Four n-channel power MOSFETs are utilized, with two MOSFETs operating on the Buck side of the LT8390A and the other two on the Boost side. The same MOSFETs as in the example circuit[39] are to be utilized. Specifically, the BSZ065NO6LS5 MOSFET will be employed for the Buck side, and the BSZ033NE2LS5 transistor for the Boost side. The suitability of the transistors sourced from the datasheet for the desired application will be evaluated.

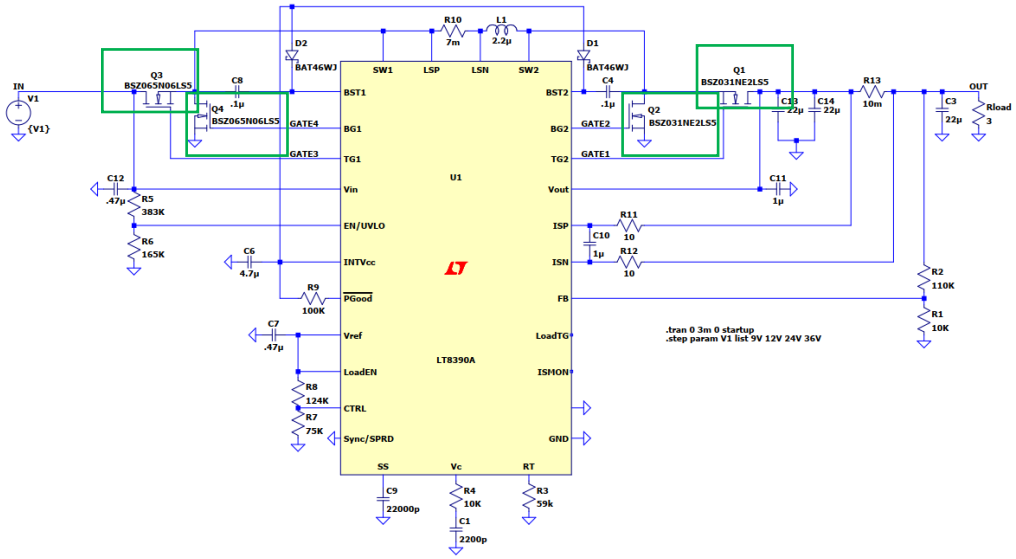


Figure 63: Integration locations of the four n-channel MOSFETS of the LT8390A, source: self-created.

The following parameters of the transistors need to be validated:

- Breakdown voltage $V_{BR(DSS)}$
- Maximum drain source current $I_{DS(MAX)}$
- Gate charge requirement Q_G

The information was obtained from the datasheets of the BSZ065NO6LS5[40] and BSZ033NE2LS5[41] transistors. Due to the change in input voltage range, only transistors Q3 and Q4 are being examined to determine if they can handle the higher input voltage. The maximum breakdown voltage $V_{BR(DSS)}$ for the BSZ065NO6LS5 (Q3, Q4) is 60 V, making them suitable for the application.

Similarly, the maximum drain-source current will significantly increase only in Q3 and Q4. The BSZ065NO6LS5 (Q3, Q4) can handle a continuous current of up to 65 A and a pulse current of 260 A. The highest current occurring in this configuration is at the drain during buck operation at 36 V.

According to Figure 64, the highest occurring current is at the drain terminal of Q3. The occurring current at 36 V is also considered since the highest voltage and thus the higher current occur during switching

[39] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 28.

[40] Cf. Infineon Technologies AG 60V (2020), Online-Source [10.3.2024] p. 1 – 9.

[41] Cf. Infineon Technologies AG (2020), Online-Source [10.3.2024] p. 1 – 9.

with a constant R_{DSON}. The peak current is approximately 17 A in the transient state and around 15 A in the steady state, which is below the $I_{DS(MAX)}$ value of the BSZ065NO6LS5.

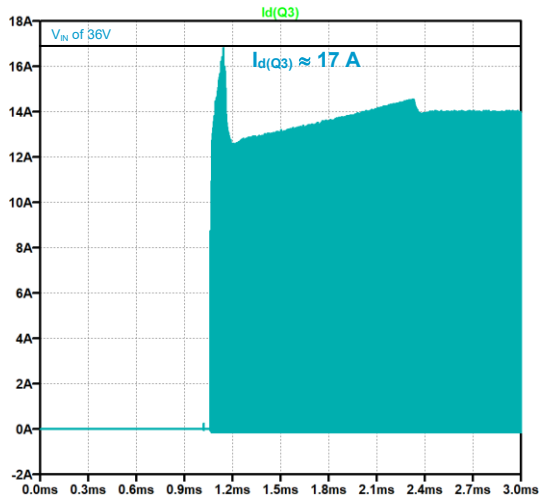


Figure 64: Drain current over the time of Q3 at 36V input voltage, source: self-created.

The gate charge requirements of Q1-Q4 are reassessed to verify if the transistors are selected within their operational limits. The MOSFETs are operated using the voltage and supplied current generated by the internal voltage regulator of the LT8390A. It is crucial that the required gate charge, depending on the switching frequency of the LT8390A, does not exceed the maximum deliverable current of the internal voltage regulator. The internal voltage regulator INT_{VCC} provides an output voltage between 4.5 V to 5 V, with a minimum deliverable current of 110 mA and a maximum of 190 mA. [42] The gate voltage range of 4.5 V to 5 V, in conjunction with the internal bootstrap circuit[43], is sufficient to drive both types of transistors. INT_{VCC} provides the necessary charge to drive the transistors. For design purposes, the minimum value of 110 mA of the INT_{VCC} is considered, as per Equation (8.6) [44] which has been adjusted regarding indices.

$$I_{INTVCC} = f \bullet (Qg1 + Qg2 + Qg3 + Qg4) \qquad (8.2)$$

I_{NTVCC}/A Gate charge current

f/s^{-1} Switching frequency

Q_{gN}/nC Gate charge

The required gate charge for BSZ065NO6LS5 (Q3, Q4) is a maximum of 13 nC, while for BSZ033NE2LS5, it is a maximum of 8.5 nC. This results in a current consumption of 86 mA at a frequency of 2 MHz, which is suitable for operational use.

[42] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 4.

[43] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 13.

[44] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 21.

8.4.1.3 Analysis of the output

Next, the generated output voltage and delivered output current will be examined. This involves measuring the voltage at the OUT node with respect to ground and measuring the current flowing through the load. (see Figure 65)

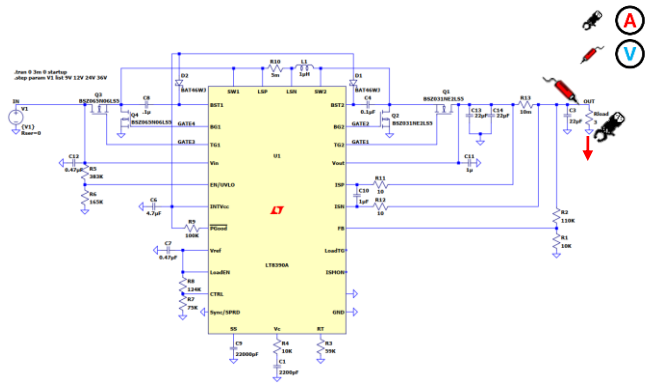


Figure 65: Measuring points for the observation of the output voltage and the output current, source: self-created.

There is a slight overshoot to around 13 V with an input voltage of 9 V. However, this is not a problem as this value remains within the tolerable limits for the devices being powered in the cell monitoring system. The occurring current and voltage ripple are also tolerably small. Therefore, there is no need to revise the output capacitances (C_{OUT}). The highest output voltage ripple occurs at an input voltage of 9V and is approximately 10mV peak-to-peak. Similarly, a peak ripple current of 3mA is observed.

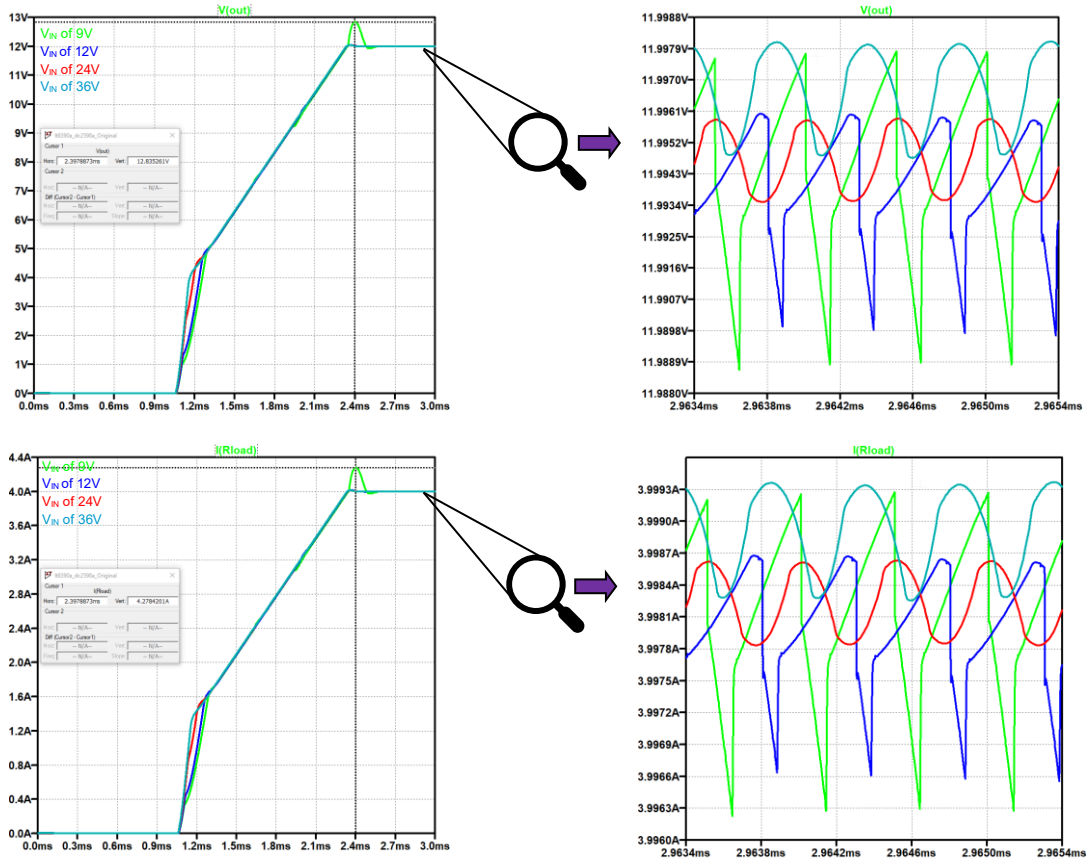


Figure 66: top left shows the output voltage curve over time, at about 2.4 ms an overshoot to 13 V occurs, top right shows the voltage ripple of the output voltage over time over all input voltage ranges. At the bottom left is the load current curve over time, whereby the load current overshoots by approximately 0.3 A due to the voltage overshoot, at the bottom right the current ripple of the load current analogue to the top right. source: both self-created.

8.4.2 Adjustments and Re-Simulation

In the redesign of inductor L_1, the ripple current will also be considered, aiming for a 50% reduction to decrease Electromagnetic interferences (EMI) load. To achieve this, a different coil type from the same product family will be chosen, as all coils in this product line are shielded, which also has a positive impact on EMI behaviour.

First, the minimum requirement for inductance will be calculated using equations[45] (8.3) and (8.4).

$$L_{BUCK} > \frac{V_{OUT} \cdot \left(V_{IN(MAX)} - V_{OUT}\right)}{f \cdot I_{OUT(MAX)} \cdot \Delta IL\% \cdot V_{IN(MAX)}} \quad (8.3)$$

$$L_{\mathrm{BOOST}} > \frac{V_{\mathrm{IN(MIN)}}^2 \cdot \left(V_{\mathrm{OUT}} - V_{\mathrm{IN(MIN)}}\right)}{f \cdot I_{\mathrm{OUT(MAX)}} \cdot \Delta IL\% \cdot V_{\mathrm{OUT}}^2} \quad (8.4)$$

L_{BUCK}/µH	inductance for the buck range
L_{BOOST}/µH	inductance for the boost range
$V_{IN(MAX)}$/V	Maximum input voltage
V_{OUT}/V	Output voltage
$V_{IN(MIN)}$/V	Minimum input voltage
$I_{OUT(MAX)}$/A	Maximum output current
$\Delta IL\%$	average-to-ripple current ratio
f/MHz	Switching frequency

With an output voltage (V_{OUT}) of 12 V, a minimum input voltage ($V_{IN(MIN)}$) of 9 V, a maximum input voltage ($V_{IN(MAX)}$) of 36 V, a maximum output current ($I_{OUT(MAX)}$) of 4 A, a switching frequency of 2 MHz, and a specified average-to-ripple current ratio of 50 %, the calculated equations yield values for L_{BOOST} of 0.75 µH and L_{BUCK} of 2 µH. Therefore, the 744377022 inductor with 2.2 µH is chosen, with a maximum ripple current ΔI_L of 10 A[46].

Adjusting the inductor L1 results in changes to the currents flowing through the current-sensing resistor R_{SENSE}, which is used for current sensing by the LT8390A and also needs to be redesigned. The occurring ripple currents are estimated using the respective equations[47] (8.5) and (8.6), and subsequently, the resistance values for the boost region and the buck region are calculated using the corresponding equations[48] (8.7) and (8.8). It is important to note that the chosen resistance values should be 20 % to 30 % lower than the calculated values of the Buck and Boost region.[49]

[45] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 20.

[46] Cf. Würth Elektronik eiSos GmbH & Co. KG 74437377022 (2021), Online-Source [1.2.2024] p. 1.

[47] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 20.

[48] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 20.

[49] Cf. ANALOG DEVICES,INC. LT8390A (2022), Online-Source [21.2.2024] p. 20.

$$\Delta IL_{(BUCK)} = \frac{V_{OUT} \cdot \left(V_{IN(MAX)} - V_{OUT}\right)}{f \cdot L \cdot V_{IN(MAX)}} \quad (8.5)$$

$$\Delta IL_{(BOOST)} = \frac{V_{IN(MIN)} \cdot \left(V_{OUT} - V_{IN(MIN)}\right)}{f \cdot L \cdot V_{OUT}} \quad (8.6)$$

$$R_{SENSE(BUCK)} = \frac{2 \cdot 50\text{mV}}{2 \cdot I_{OUT(MAX)} + \Delta IL_{BUCK}} \quad (8.7)$$

$$R_{SENSE(BOOST)} = \frac{2 \cdot 50\text{mV} \cdot V_{IN(MIN)}}{2 \cdot I_{OUT(MAX)} \cdot V_{OUT} + \Delta IL_{BOOST} \cdot V_{IN(MIN)}} \quad (8.8)$$

$\Delta IL_{(BOOST)}$/A Ripple current of the boost range

$\Delta IL_{(BUCK)}$/A Ripple current of the buck range

L /µH Inductance of L_1

f/MHz Switching frequency

$V_{IN(MAX)}$/V Maximum input voltage

V_{OUT}/V Output voltage

$V_{IN(MIN)}$/V Minimum input voltage

$I_{OUT(MAX)}$/A Maximum output current

$R_{\text{SENSE(BUCK)}}$/mΩ Resistance for the buck range

$R_{\text{SENSE(BOOST)}}$/mΩ Resistance for the boost range

The peak-to-peak ripple currents in the boost region amount to 0.51 A and approximately 1.82 A in the buck region. These results are used for designing the current-sensing resistors. With a $\Delta I_{L(BOOST)}$ of 0.51 A and ΔI_{LBUCK} of 1.82 A, an R_{SENSE} boost of around 8.81 mΩ and an $R_{SENSE(BUCK)}$ resistance value of approximately 10.183 mΩ are derived. Taking into account the requirement that the resistors should be chosen 20 % to 30 % smaller, the values for $R_{SENSE(BOOST)}$ range from 6.17 to 7.05 mΩ, and correspondingly for $R_{SENSE(BUCK)}$ from 7.13 to 8.14 mΩ. The R_{SENSE} resistor selected is the WSL2512 with 6 mΩ, 0.5 % tolerance, and 1 W rated power. The value for the boost was determined based on the higher continuous current set across the inductor in the boost region.

8.4.3 Simulation and analysis of modified circuit

The updated components have been incorporated into the simulation circuit, and the simulation has been run again. This process validated the newly designed inductor L1 regarding the occurring currents, determined the maximum current through R_{SENSE}, and assessed the resulting power loss. Building upon the simulation results, the output voltages and currents were verified at both 9 V and 36 V input levels.

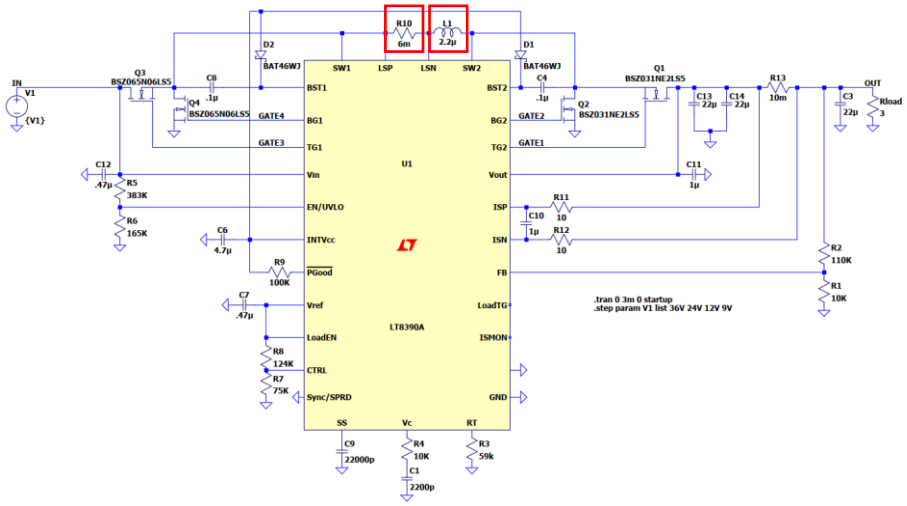


Figure 67: Adapted simulation circuit of the LT8390A with the new values for R_{SENSE}(R10) and the storage inductor L1, source: own illustration.

Based on the diagram, the maximum occurring inductor current can be determined across all four input voltages. At 9 V input, a current spike of around 9.4 A occurs after 2.35 ns. Regarding the storage inductor L1 (744377022), the saturation current is not reached and is therefore permissible. The peak current of 9.4 A generates a momentary power loss of around 530 mW across R_{SENSE} (R10) (I^2L1*R_{SENSE}), which is below the limit of 1 W and is thus also permissible.

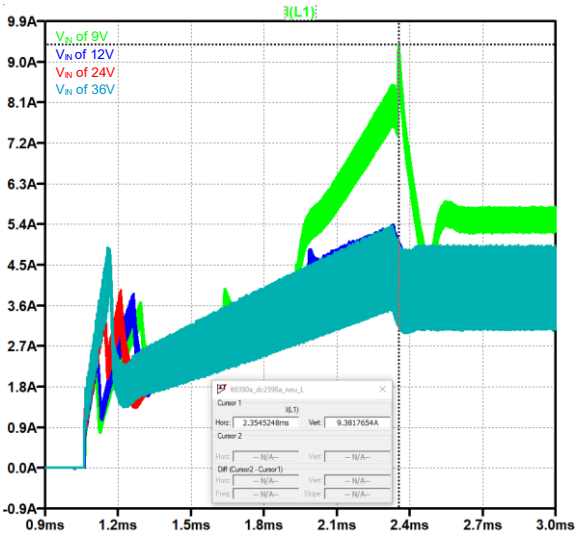


Figure 68:The inductor currents across L1 over time, with different input voltages, source: self-created.

Based on Figure 69, it is determined that the specified output parameters of 12 V output voltage and a 4 A output current are achieved. Although there is some overshoot at a 9 V input voltage, as mentioned earlier in 8.4.1.3 on page 58, it is not a problem for the enlarged components.

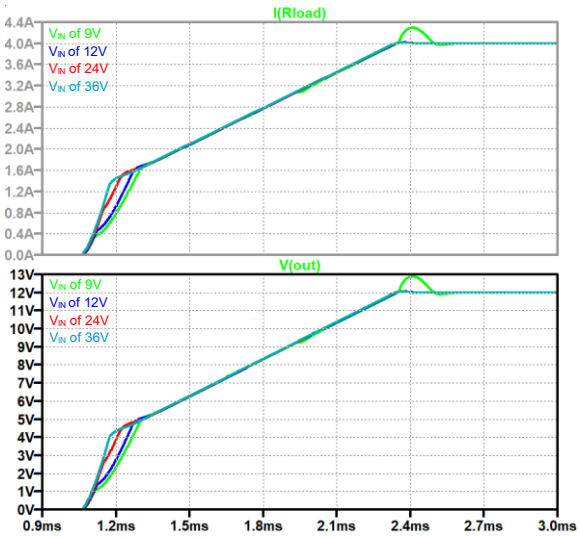


Figure 69:Top: transient behaviour of the output current over time, bottom: transient behaviour of the output voltage over time, source: self-created.

8.4.4 Design of the input capacitors

The simulation in section 8.4.3 is first expanded to include components from the LTC4368 circuit. Specifically, the effective R_{DSON} values of the transistors and the resistance value of the current sensing resistor of the LTC4368 are incorporated into the simulation to obtain a more realistic representation of the circuit assembly. This will aid in designing the input capacitance of the LT8390A.

8.4.5 Design of LTC4368

The LTC4368 serves as a protection IC for the LT8390A. It provides overvoltage (*OV*) and undervoltage (*UV*) protection, as well as overcurrent (*OC*) and reverse current (*RC*) protection. To set the necessary limits for *OV*, *UV*, *OC*, and *RC*, the LTC4368 is externally connected with resistors and capacitors. Transistors are used as switching elements. Figure 70 shows an example circuit.

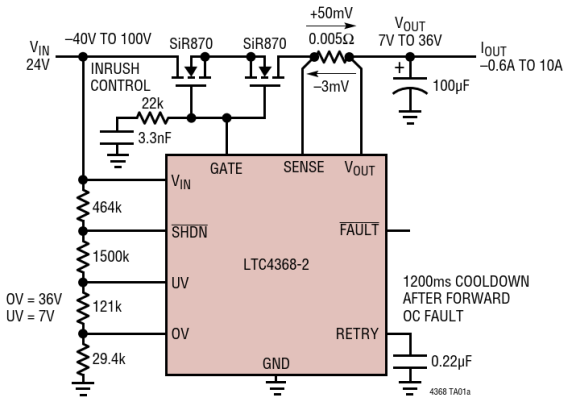


Figure 70: Example circuit of the LTC4368 for a 24 V application as a circuit breaker of 10 A, source: ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 1.

8.4.5.1 Setting the supply voltage hysteresis

The threshold values for the resistive components connected to *UV* and *OV* are calculated using the equations[50] (8.9) to (8.12), where the worst-case leakage current I_{UV} is 10 nA[51] and the maximum allowable offset voltage ($V_{OS(UV)}$) at the *UV* pin should be 0.1 mV.

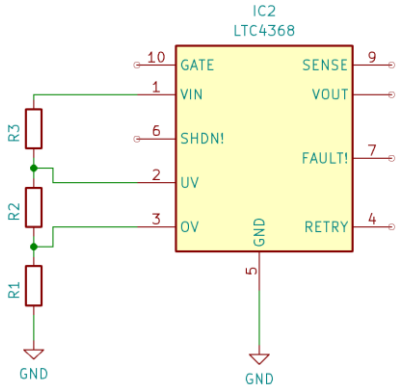


Figure 71: Wiring of *UV* and *OV* pins via the voltage input V_{IN} of LTC4368, source: own Illustration.

$$R_1 + R_2 = \frac{V_{OS(UV)}}{I_{UV}} \quad (8.9)$$

$$R_3 = \frac{V_{OS(UV)}}{I_{UV}} \cdot \left(\frac{UV_{TH} - 0.5\text{V}}{0.5\text{V}}\right) \quad (8.10)$$

$$R_1 = \frac{\left(\frac{V_{OS(UV)}}{I_{UV}}\right) + R_3}{OV_{TH}} \cdot 0{,}5\text{V} \quad (8.11)$$

$$R_2 = \frac{V_{OS(UV)}}{I_{UV}} - R_1 \quad (8.12)$$

$R_1 - R_3/\Omega$	Resistors values
$V_{OS(UV)}/\text{mV}$	Offset voltage of UV
I_{UV}/nA	Leakage current
UV_{TH}/V	Undervoltage threshold
OV_{TH}/V	Overvoltage threshold

With an *OV* threshold of 36 V and an undervoltage threshold of 9 V, the values for *R1* are 25 kΩ, for *R2* are 75 kΩ, and for *R3* they amount to 1.7 MΩ. The SHDN! pin controls the activation of the GATE charge pump for the external MOSFETs. A high level (SHDN! high) activates the pump, while a low level (Low) puts the LTC4368 into low-current mode. In case of overcurrent, the SHDN! pin needs to be briefly toggled low and then high to re-enable the charge pump. The voltage on the SHDN! pin must not exceed 80 V when V_{IN} is above 80 V.[52]Therefore, the resistor *R3* is divided to ensure that the voltage at SHDN! does not exceed 80 V, provided that the maximum permissible 100 V[53] for V_{IN} is not exceeded.

[50] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 12.

[51] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 4.

[52] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 7.

[53] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 3.

The resistance value of *R3* is divided, and the value for *R4* is calculated using the voltage divider rule. *R3* is split into two resistors, *R3a* and *R3b* (see (8.9)). Substituting *R3a* with *R3* – *R3b* and solving for *R3b* (8.10) yields the value of *R4*, as per the voltage division principle.

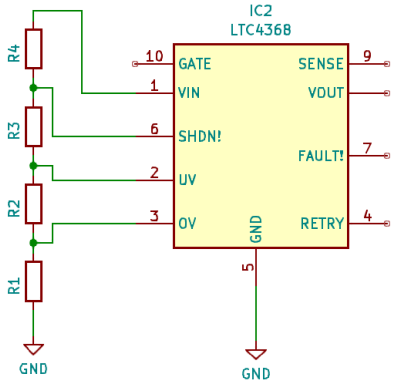


Figure 72: LTC4368 wiring considering the SHDN! pin voltage rating, Source: own Illustration.

$$\frac{U_{TOTAL}}{R_1 + R_2 + R_{3a} + R_{3b}} = \frac{U_{3b}}{R_{3b}} \quad (8.13)$$

$$R_{3b} = \frac{U_{3b} \cdot (R_1 + R_2 + R_3)}{U_{TOTAL}} \quad (8.14)$$

$R_1 - R_{3b}/\Omega$ Resistors values

U_{TOTAL}/V Total voltage

U_{3b}/V Voltage over R_{3b}

For a total voltage U_{TOTAL} of 100 V, a partial voltage of 20 V, and resistance values of 25 kΩ (*R1*), 75 kΩ (R2), and 1.7 MΩ (R3), the value for R4 (R3b) is calculated to be 360 kΩ.

Therefore, based on the 360 kΩ value of R4(R3b), the value for R3 is calculated to be 1.34 MΩ. Since a resistance value of 1.34 MΩ is not available as a physical component, a 1.33 MΩ resistor is used for *R3*, while a 370 kΩ resistor is chosen for *R4*. This arrangement ensures that the voltage at the SHDN pin remains below 80 V as long as the total voltage does not exceed 100 V. The calculated values for *R1* and *R2* remain unchanged.

8.4.5.2 Overcurrent fault setting

In order to set the threshold for the overcurrent (*OCTH*), it is necessary to estimate the current drawn by the LT8390A through the drain terminal of Q3. Since decoupling capacitors are still installed, the input current ($I_{Q3(DRAIN)}$) exhibits a high ripple. Therefore, the RMS current value is used as an estimation for *OCTH* adjustment, based on simulation results. The highest current ripple is observed at a 36 V input voltage, but the highest total current occurs during Boost operation, hence at a 9 V input voltage.

To capture the RMS value, the built-in functionality of LTspice was utilized. The time axis was adjusted to align the start time value with the beginning of the Q3 switching cycles. Since the current value is 0 before that point, performing an RMS calculation over the entire simulation time (0 ms to 3 ms) would distort the result.

Based on Figure 73, it can be observed that an RMS current of approximately 4.6 A occurs within the time interval from 2.26 ms to 2.35 ms as the highest currents occur during this period due to the LT8390A's transient phase. The highest occurring RMS residual current is around 7 A therefore, an overcurrent threshold of 8 A minimum is defined.

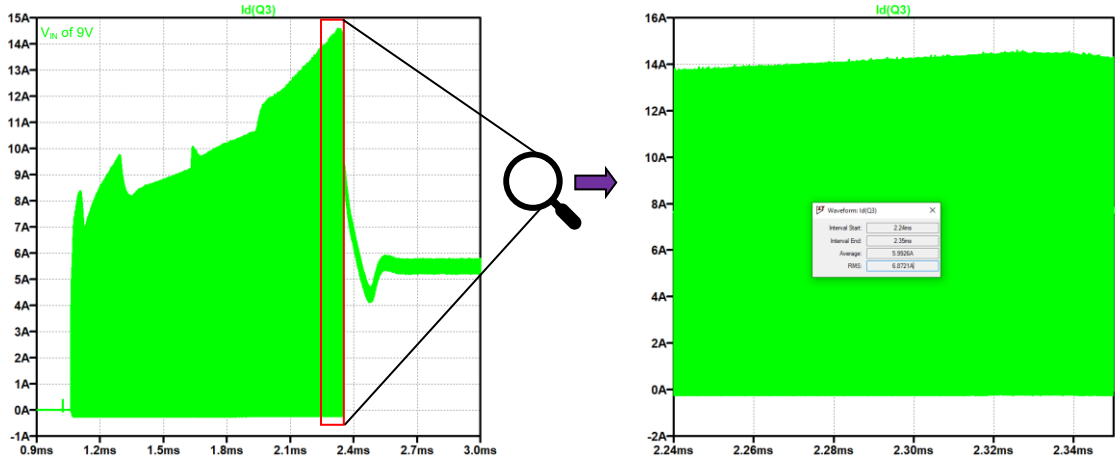


Figure 73: Current profile over time at Q3 drain terminal, Source: own Illustration.

This provides the opportunity to determine the current sensing resistor installed between the SENSE pin and V_{OUT}, which sets the overcurrent threshold I_{OCFWD}, and thus R_{SENSE} can be calculated.(8.15)[54]

$$I_{OC,FWD} = \frac{50\ \text{mV}}{R_{SENSE}} \tag{8.15}$$

$I_{OC,FWD}$/A Overcurrent threshold

R_{SENSE}//mΩ Current sensing resistor value

Therefore, the value of R_{SENSE} is determined to be 6 mΩ. A shunt resistor with a value of 6 mΩ and a permissible power dissipation of 1 W was selected. It is noted that the actual power dissipation is around 417 mW. By choosing a 6 mΩ resistor, a forward overcurrent threshold of around 8.33 A and a reverse current threshold of approximately -0.5 A is established.(8.16)[55]

$$I_{OC,REV} = \frac{\text{-3 mV}}{R_{SENSE}} \tag{8.16}$$

$I_{OC,REV}$//A Reverse current threshold

R_{SENSE}/mΩ Current sensing resistor value

[54] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 13.

[55] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 14.

8.4.5.3 Selection of transistor

The transistors used on the buck side are the BSZ065NO6LS5. These transistors have a typical R_{DSON} of 6.5 mΩ[56]. Therefore, with the current sensing resistor R_{SENSE} calculated previously, the total series resistance for the LT8390A amounts to 19 mΩ.

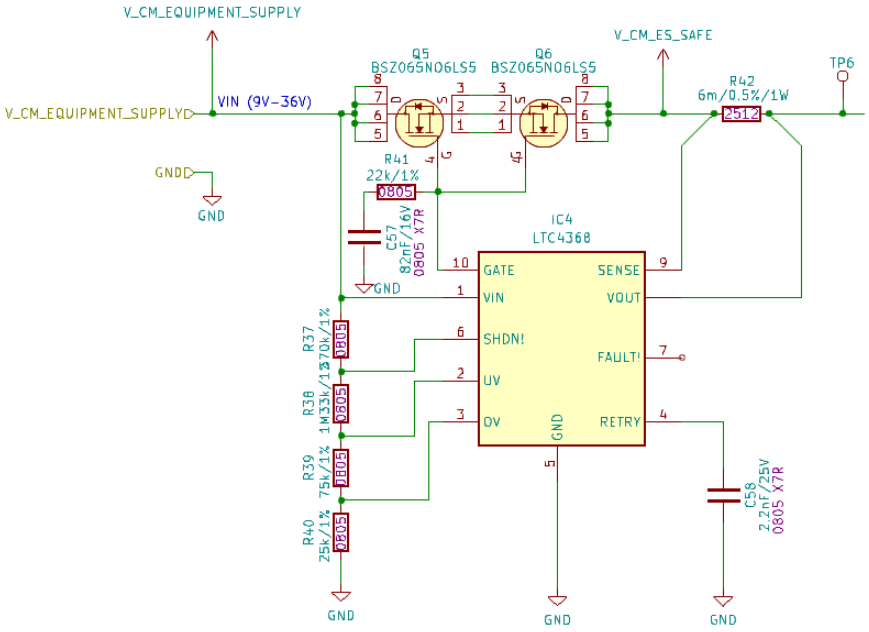


Figure 74: Minimum wiring of the LTC4368, source: self-created.

To adjust the inrush current limiting of the LTC4368, it is necessary to design the input filter capacitors at the input of the LT8390A beforehand.

[56] Cf. Infineon Technologies AG 60V (2020), Online-Source [10.3.2024] p. 1.

8.4.6 Selection of input capacitors

The largest ripple current occurs at an input voltage of 36 V, which serves as the basis for designing the input capacitors. To determine the required capacitance, the maximum ripple current is evaluated from the simulation data. Given the 2 MHz switching frequency, the signal period is 500 ns. The smoothing capacitor is intended to supply the necessary charge during the Q3's turn-on time. This turn-on time was measured from the simulation data and is approximately 60 ns.

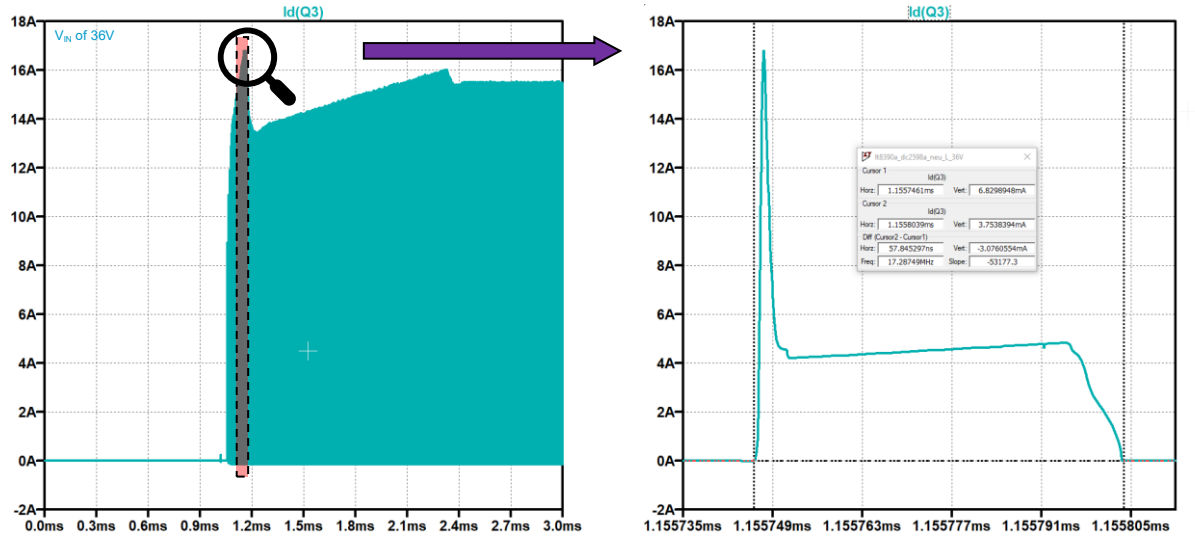


Figure 75: Left: Current waveform of *Id(Q3)* over time with marked zoom area. right: Zoomed-in section with cursor time measurement of the turn-on time, source: self-created.

The required capacitance is calculated using Equation (8.17), where ΔU represents the allowable voltage change across the capacitor, and the integral in the denominator calculates the charge to be delivered during the voltage change.

$$C = \frac{1}{\Delta U} \int_{t1}^{t2} i_{d(Q3)} \cdot dt \qquad (8.17)$$

C/F Capacitance

ΔU/V Permissible voltage drop

$i_{d(Q3)}$/A Charging current

The calculation is implemented using Matlab, where the data generated by LTspice was processed in Matlab as a text file. The calculation results in a charge Q value of approximately 260 nC for one switching cycle at 36 V input voltage. (Figure 76)

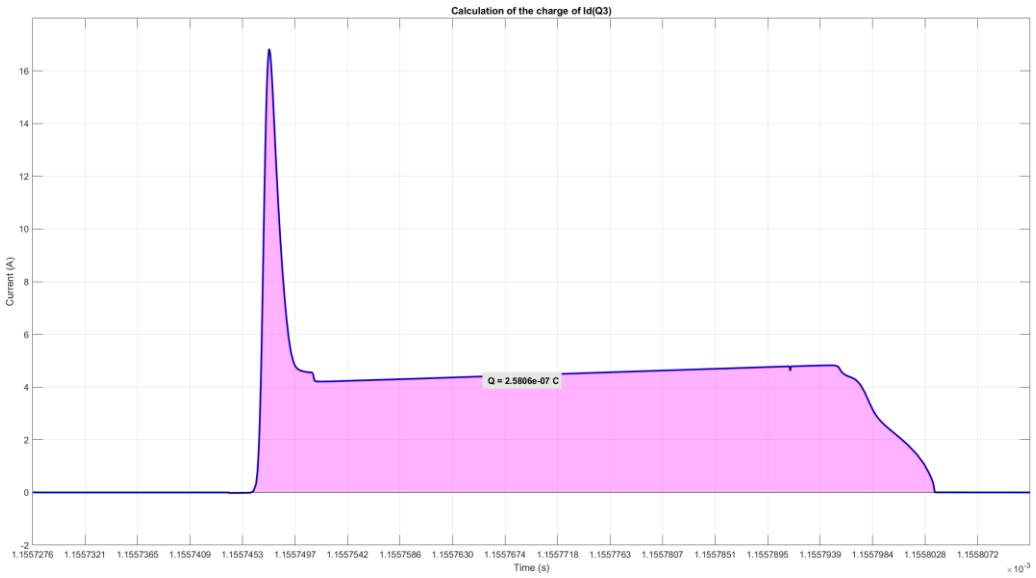
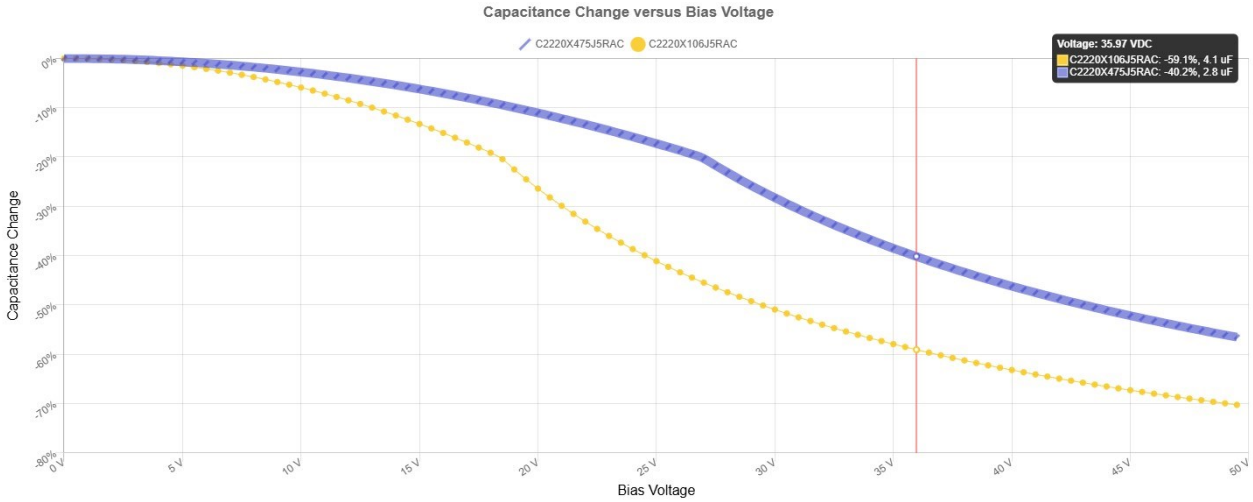


Figure 76: Drain current of Q3 over time within one switching period at 36 V input voltage, source: self-created.

Based on this charge quantity, the smoothing capacitors are designed. The development goal is to achieve a low ripple voltage to prevent EMI and potential effects on other circuit parts. The ripple voltage or permissible voltage drop should be 0.01 V.

This results in a total capacitance of around 26 µF. For these purposes, X7R ceramic capacitors are used. The 26 µF is achieved by connecting one 10 µF capacitor and three 4.7 µF capacitors in parallel. The reason for this configuration is twofold: firstly, the ripple current load is distributed across multiple capacitors, reducing the strain on any single capacitor; secondly, the smaller size of the individual capacitors results in lower parasitic inductance, allowing the stored charge to be released more quickly, which improves smoothing. Additionally, paralleling the capacitors reduces the Equivalent Series Resistance (ESR).

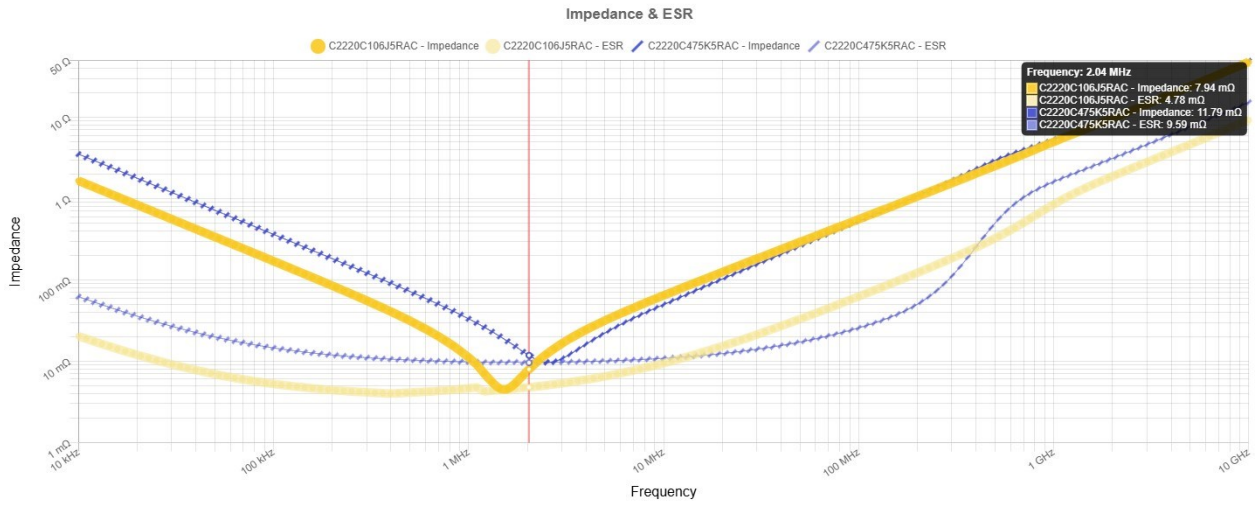
DC bias needs to be considered for ceramic capacitors, and the maximum allowable ripple current for all capacitors must be observed. It is also essential to ensure that a minimal ESR is maintained at 2 MHz. From Figure 77, it can be observed that at 36 V, the 4.7 µF capacitor exhibits a residual capacitance of 2.8 µF due to the DC bias effect. For instance, the 10 µF capacitor may effectively provide only 4.1 µF under the influence of DC bias. As a consequence, an additional 4.7 µF and 10 µF capacitor are installed.



Legend	Tolerance	Part Number	Cap.	V_{DC}*	Dielectric	Qty.	Bias (V)	Amb. (°C)
	5%	C2220X106J5RAC	10 uF	50	X7R	1	0	25
	5%	**C2220X475J5RAC**	**4.7 uF**	**50**	**X7R**	1	0	25

Figure 77: Impact of the DC bias effect on the selected ceramic capacitors using a simulation tool, source: KSIM3 from KEMET Corporation (2021), Online-Source [1.4.2024].

Figure 78 shows the behaviour of the ESR and impedance of the capacitors over frequency. The figure indicates that both ESRs reach their minimum in the frequency range from 1 MHz to 3 MHz. Since the ripple frequency is at 2 MHz, both types are suitable for use as smoothing capacitors in terms of ESR. The yellow graphs show the impedance and ESR of the 10 µF capacitor, while the blue graphs show those of the 4.7 µF capacitor.



Legend	Tolerance	Part Number	Cap.	V_{DC}*	Dielectric	Qty.	Bias (V)	Amb. (°C)
	5%	C2220C106J5RAC	10 uF	50	X7R	1	0	25
	10%	C2220C475K5RAC	4.7 uF	50	X7R	1	0	25

Figure 78: Frequency behaviour of the ESRs and impedances of the selected ceramic capacitors, source: KSIM3 from KEMET Corporation (2021), Online-Source [1.4.2024].

The simulation in KSIM3 is repeated, with all capacitors (four 4.7 µF and two 10 µF) acting in parallel to each other, just as in the actual application. The simulation result (gray graph), depicted in Figure 79, illustrates the overall ESR and impedance characteristics of the capacitor assembly. This yields a total ESR and impedance of 2.3 mΩ.

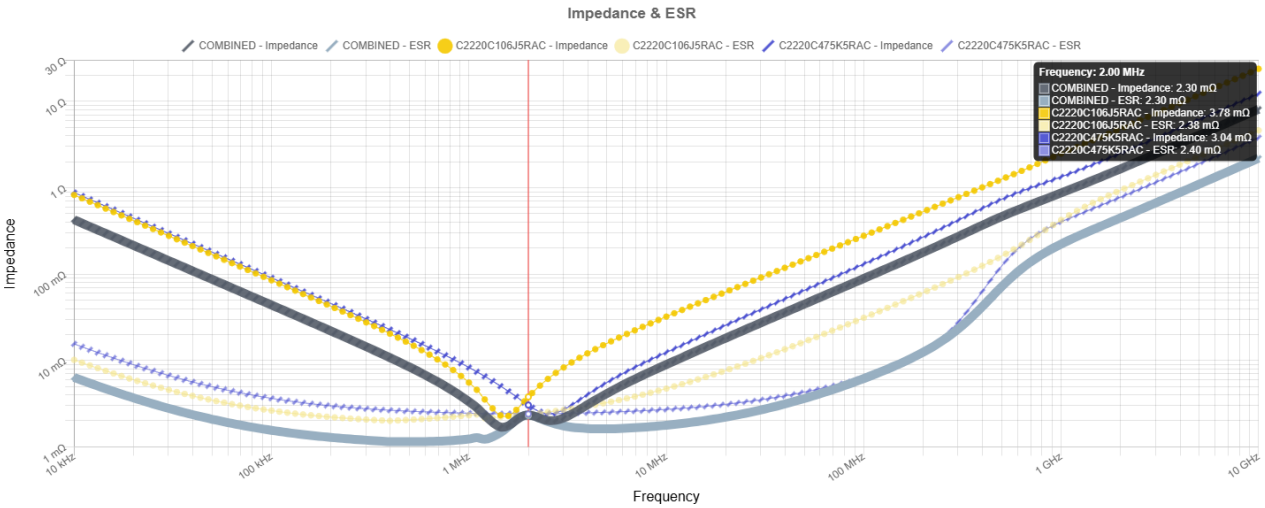


Figure 79: Frequency behaviour of the entire circuit's ESRs and impedances of the selected ceramic capacitors, KSIM3 from. KEMET Corporation (2021), Online-Source [1.4.2024]

All models[57] of the capacitors have been added to the simulation circuit (Figure 80). Additionally, a 5-meter-long copper connection line was modelled by adding a resistor and an inductor. This results in a total of 10 m for the outgoing and return line. A 113 mΩ (R15) resistor, with a specific resistance of 0.0169 Ωmm²/m for copper, and a 1250 nH inductance (L2) based on 250 nH/m of a coaxial cable, were

[57] Cf. KEMET Corporation (2021), Online-Source [1.4.2024]

integrated into the circuit. While the voltage supply in the real setup is made using ordinary copper wires, the inductance of the coaxial cable serves as the minimum inductance value. Furthermore, the R_{DSON} (R14) and current sensing resistor of the LTC4386 were set to a total of 19 mΩ. This ensures that the simulation provides more realistic values for the influence of the ripple voltage by the capacitors. The simulation data is used both to estimate the final input ripple current and to determine the ripple current occurring at the capacitors.

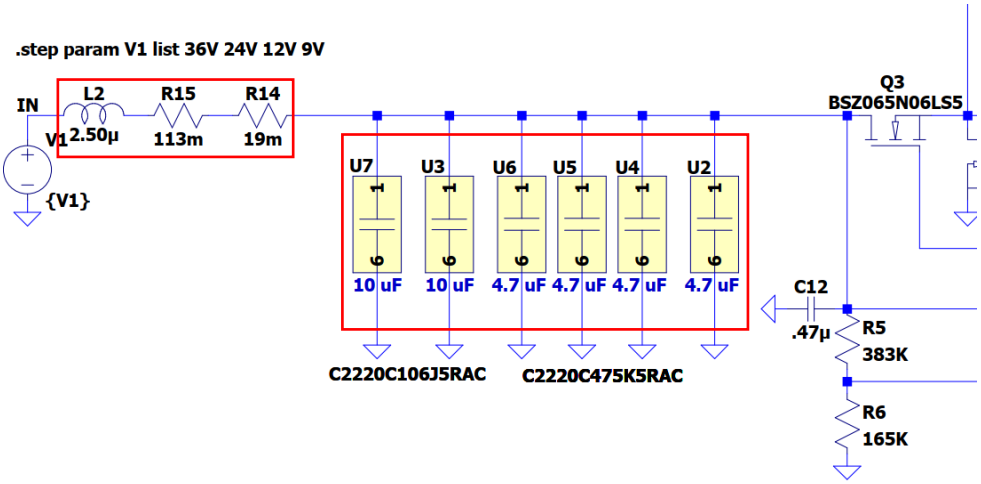


Figure 80: Simulation circuit expanded with input capacitors and internal resistance of the voltage source, source: self-created.

The simulation provides the following results for the total input ripple current and voltage, as well as for the individual capacitances. The current was measured across R14 using a current probe, and the voltage before the capacitors (Figure 81) was recorded.

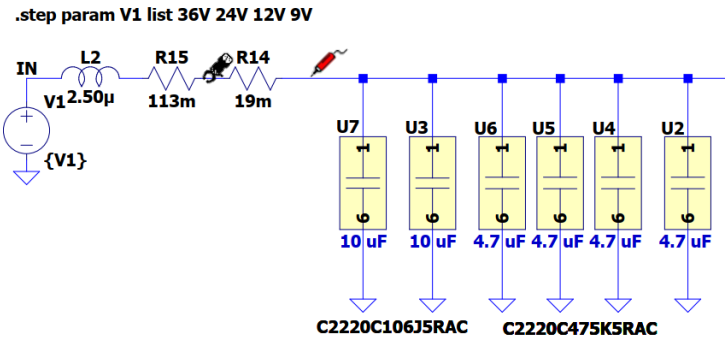


Figure 81: Measuring point for recording the total input current and voltage, source: self-created.

Figure 82 on the left, shows the input currents for 9 V, 12 V, 24 V, and 36 V. The highest current value occurs during the transient response at a supply voltage of 9 V. However, it does not exceed the overcurrent threshold of the LTC4368 and is thus permissible.

Figure 82 on the right depicts the voltage waveform of the measurement point under Figure 81 for 9 V, 12 V, 24 V, and 36 V source voltage. Neither current nor voltage show significant ripple, thus the capacitors can be incorporated into the circuit design.

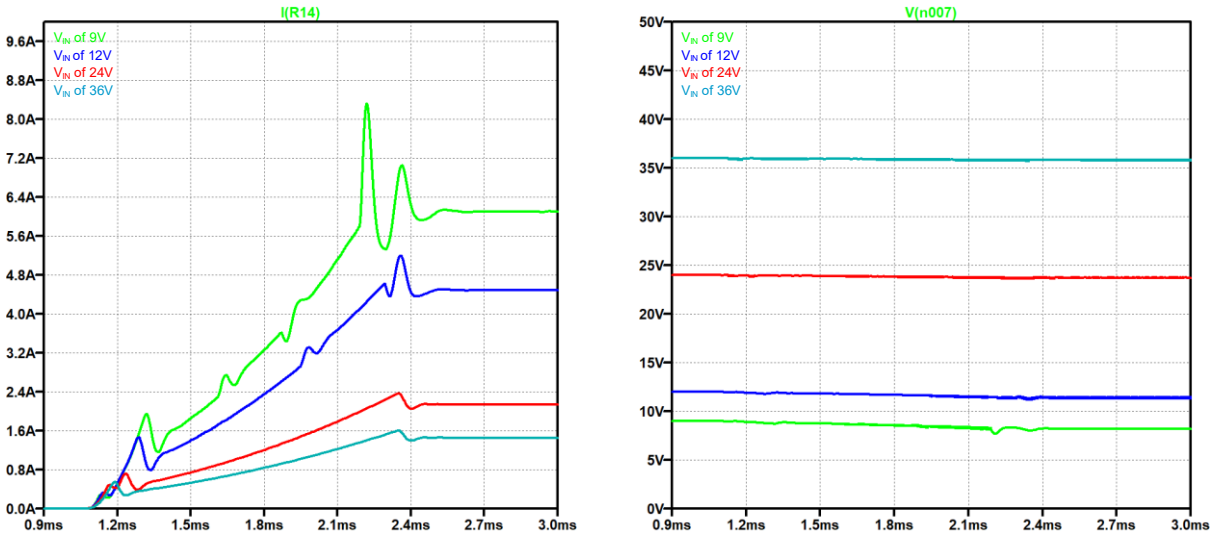


Figure 82: Left: current waveform across R14, right: voltage waveform at the measurement point at full load, source: self-created.

In Table 3, the simulation results for the individual input capacitances are depicted. The first column indicates which capacitor was considered. The second column shows the simulation results of the respective capacitors for an input voltage of 9 V, while the results for an input voltage of 36 V are presented in the third column.

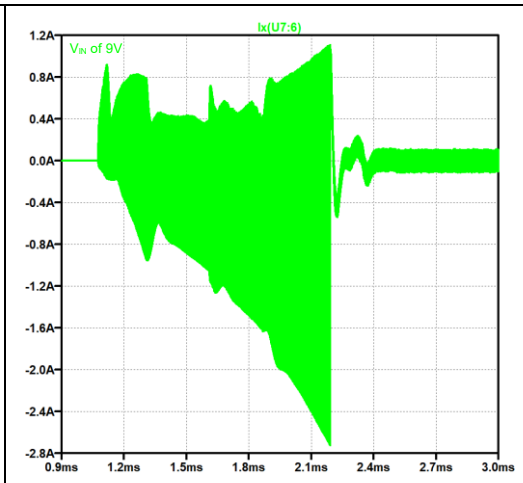
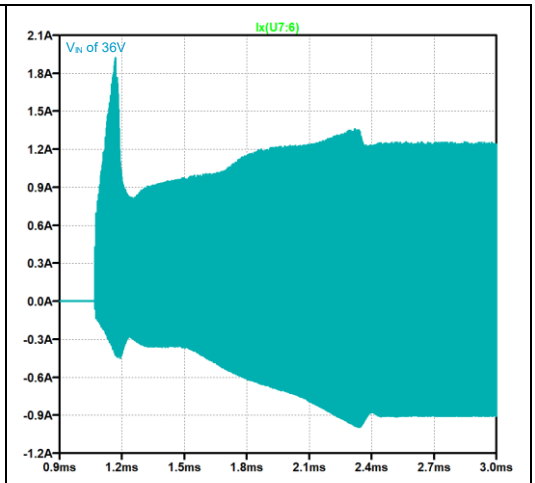
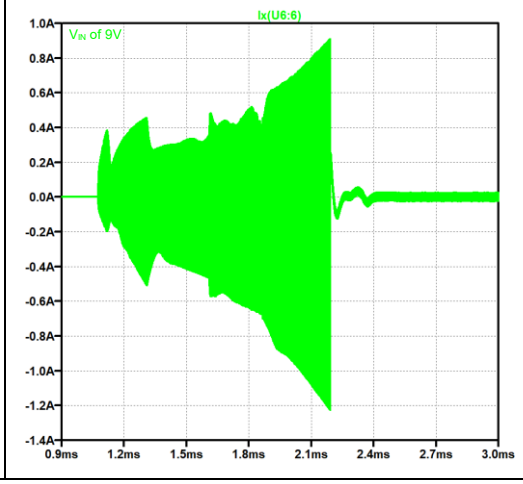
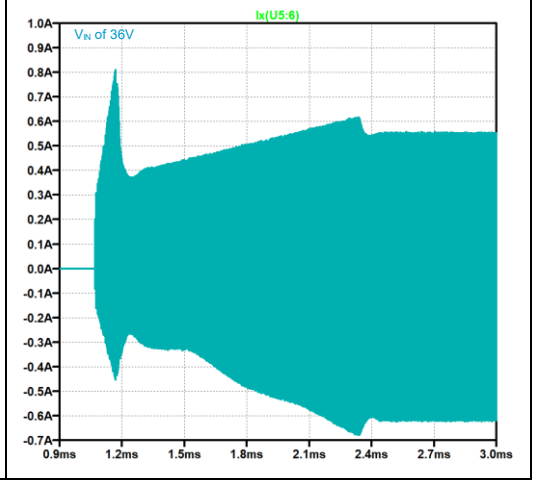
U7, U8		
U6, U5, U4, U2		

Table 3: Ripple currents of the individual input capacitors for 9 V input voltage (left) and for 36 V input voltage (right), source: self-created.

For all capacitors, X7R 1210 ceramic types are used. The maximum allowable ripple current, along with the heating effect, is illustrated in Figure 83 and Figure 84. For the 10 µF capacitors, peak-to-peak ripple currents of approximately 400 mA (Table 3 top left) are observed in the steady state. In the transient region, current spikes of up to around 2.8 A occur at a 9V input voltage. With a 36 V (Table 3 top right) input voltage, a continuous ripple of 2.1 A peak-to-peak is established. Regarding the 4.7 µF (Table 3 top left and right) capacitors, transient current spikes of 1.2 A are observed at a 9 V input voltage, with a continuous ripple current of approximately 200 mA peak-to-peak. With a 36V input voltage, a continuous ripple current of 1.2 A peak-to-peak is established.

Figure 83 and Figure 84 show the relationship between temperature rise and ripple current at 2 MHz. It can be observed that the capacitors only experience a slight temperature increase at the ripple currents determined by the simulation. Therefore, both types are suitable for this utilisation.

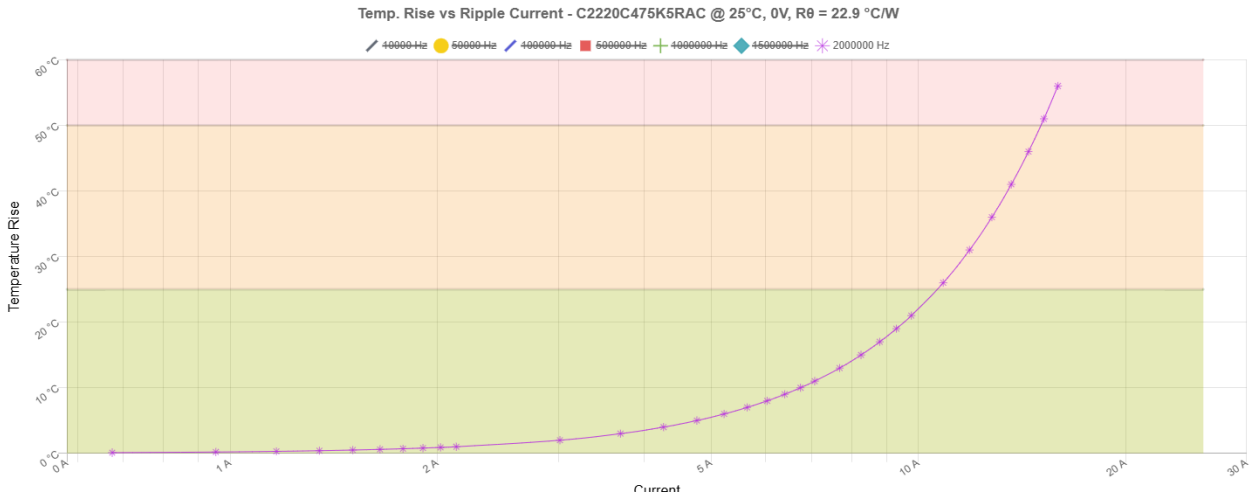


Figure 83: Temperature increase via the effective ripple current at different frequencies of the 4,7 µF capacitors, source: KSIM3 from KEMET Corporation (2021), Online-Source [1.4.2024].

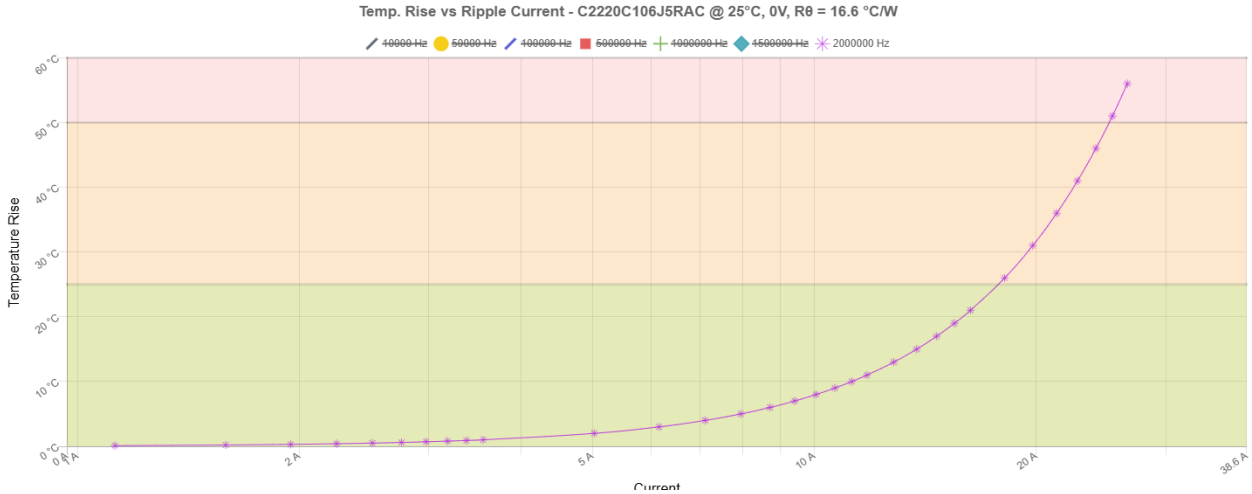


Figure 84:Temperature increase via the effective ripple current at different frequencies of the 0,27 µF capacitors, source: KSIM3 from KEMET Corporation (2021), Online-Source [1.4.2024].

8.4.7 Activation of the voltage regulator

The voltage regulator is delayed activated to allow for charging of the input capacitors without the LT8390A being operational. This is achieved by selectively activating the EN/UVLO pin of the LT8390. A comparator implemented with an operational amplifier is utilized for this purpose. The voltage V_CM_ES_SAFE is tapped after the transistors of the LTC4860 (see Figure 85).

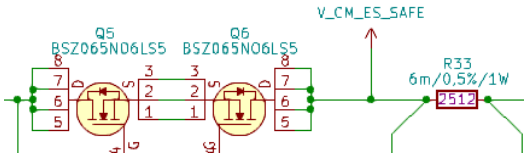


Figure 85: Tap point of the V_CM_ES_SAFE for operation as well as comparative voltage of the comparator, source: own illustration.

The mentioned voltage, V_CM_ES_SAFE, serves both as a supply for the LT6015 and as a reference voltage through the voltage divider R43 and R44. The non-inverting input of the comparator is connected to an RC circuit with a time constant of $\tau = 0.2$ s. Through the division ratio of the voltage divider, a voltage of 95 % of the input voltage is reached at the inverting input of the comparator. After three times τ (0.6 s), the voltage across capacitor C62 reaches 95 % of the input voltage, causing the operational amplifier to switch its output from GND to V_CM_ES_SAFE, thereby activating the LT8390A. This mechanism ensures that the capacitors are mostly charged before the voltage regulator begins its operation.

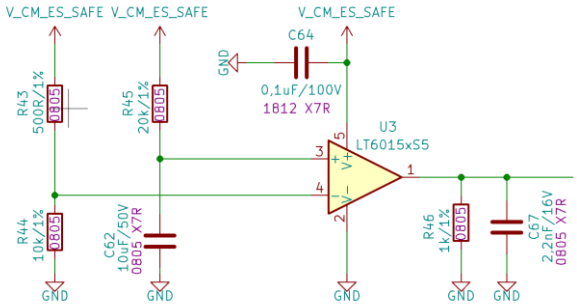


Figure 86: Comparator circuit for time-delayed activation of the LT8390A, source: own illustration.

8.4.8 Inrush current limiting

The inrush current limiting is implemented by the LTC4368 by connecting a capacitance to the gate pin in combination with a resistor. Refer to a sample circuit from the datasheet in Figure 87 for illustration.

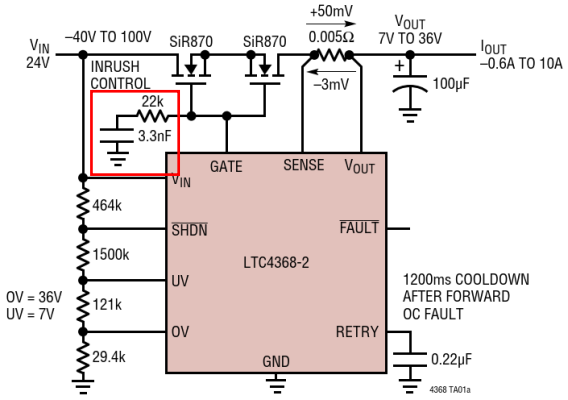


Figure 87:Example circuit of the LTC4368 for a 24 V application as a circuit breaker of 10 A, source: adopted ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 1.

Since the LT8390 is only started after 0.6 s and no operating current flows during this time, there is no need for extensive effort regarding inrush current limitation. The inrush current should be limited to a maximum of 6 A.

$$I_{\mathrm{INRUSH}} = \frac{C_{\mathrm{OUT}}}{C_{\mathrm{GATE}}} \cdot I_{\mathrm{GATE(UP)}} \tag{8.18}$$

I_{INRUSH}/A Possible inrush current

C_{GATE}/F Gate capacity

C_{OUT}/F Output capacity

$I_{\mathrm{GATE(UP)}}$/A Gate charge current

By rearranging equation (8.18), a value of 137.15 µF is obtained for C_{OUT} and a maximum inrush current of 6 A requires a C_{GATE} of approximately 80 nF when $I_{GATE(UP)}$ is 35 µA[58]. An 82 nF capacitor is chosen for C_{GATE}. The 22 kΩ resistor is taken from the example circuit. The FAULT! function is not required and therefore not connected anywhere. The RETRY pin is connected to a 2.2 nF capacitor to GND. This triggers an automatic retry after an error event, with the LTC4368 waiting for 12.1 ms before reactivating through the 2.2 nF capacitor. [59]

[58] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 4.

[59] Cf. ANALOG DEVICE,INC LTC4368 (2021), Online-Source [22.02.2024] p. 13.

8.4.9 Remaining circuit Implementation

LOADTG is the inverted and buffered input signal of **LOADEN** and is not used; therefore, this pin remains unconnected.

The **Test** pin is utilized for factory testing and must be directly connected to GND, as it is not needed for further operation.

The **ISMON** pin allows for parallel operation of multiple LT8390A devices, but since this function is not required, the pin is left unconnected.

The **CTRL** pin is used to limit the input or output current, with values directly taken from the example circuit.

LOADEN allows for the external control of the high-side switches; however, as this function is not needed, this pin is directly connected to the **VREF** pin. The **VREF** pin provides a reference voltage necessary for the operation of the LT8490A, requiring an external capacitor for the reference voltage source. The necessary capacitance is taken from the example circuit.

The soft start function, realized through the **SS** pin, can be utilized to implement various fault protection modes, with an additional recommendation to connect a 22 nF capacitor. As the hiccup mode is chosen as the fault protection mode, no additional circuitry is required.

The **VC** linkage compensates the control loop of the LT8390A, requiring an RC network to be connected, with values taken from the example circuit.

The **FB** pin provides the feedback voltage of the target voltage and determines the output voltage to be generated, with values of the voltage divider taken from the example circuit.

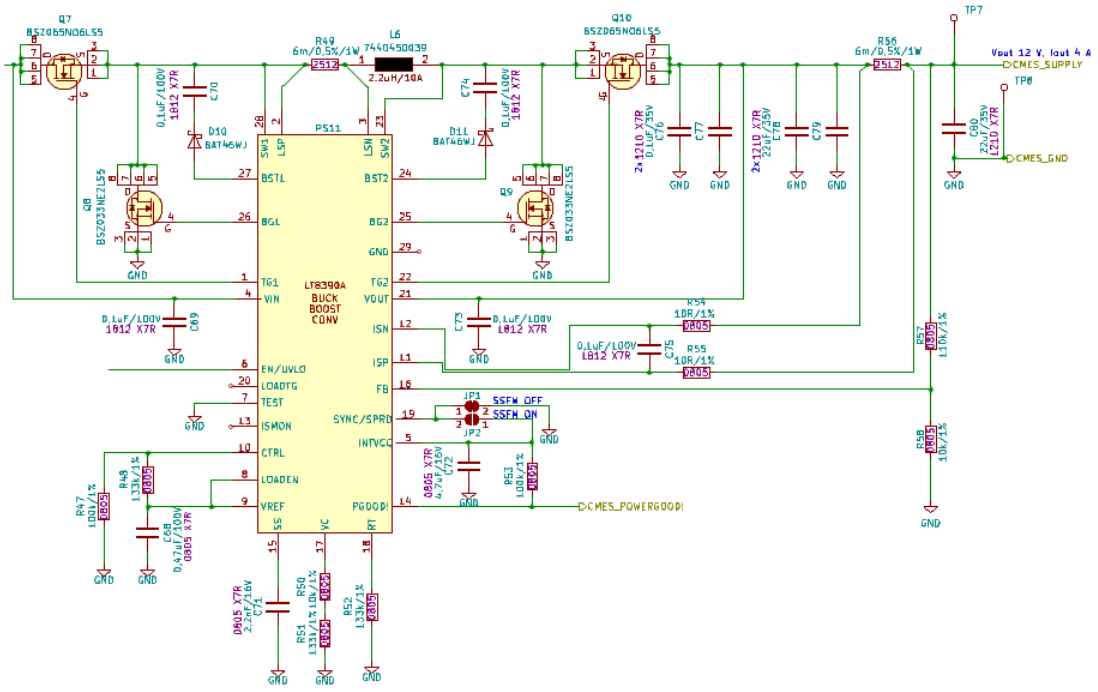


Figure 88: The fully implemented LT8390A with all the required subcircuits, source: own illustration.

8.5 Cell probe voltage supply

The "Cell Probe Voltage Supply" block powers the control electronics of the cell probe and has been directly taken from the old schematic. This block provides 250 mA at +/-3 V, 1 A at +5 V, 1 A at +3.3 V, and 500 mA at +/-15 V. A DC-DC converter is employed, which converts the input voltage from 9 V to 36 V to the +/-15 V, serving as the starting point for the other voltage regulators. The power requirement of the circuit block at the input side is approximately 16.85 W with an efficiency of 89 % of the DC-DC converter.

8.6 Cell probe voltage supply isolated

The Cell Probe Voltage Supply Isolated block has also been adopted from the old schematic. As the name suggests, this supply block is galvanically isolated from the other supplies and is used to power the voltage measurement, where significantly higher voltages (up to 1000 V) can occur. The input voltage is provided by the +/-15 V regulator of the cell probe voltage supply. The Cell Probe Voltage Supply Isolated block provides 250 mA at +/-3 V, 1 A at 5 V, 50 mA at +/-12 V, 1 A at +3.3 V, and 133 mA at +15 V.

8.7 Cell probe current sensor supply

The fluxgate current sensors receive their power supply from the circuit block "Cell Probe Current Sensor Supply." Since fluxgate current sensors from LEM are preferred, the product portfolio was reviewed in terms of current measurement range, supply voltage, supply current, and accuracy. Only sensors with an accuracy of at least 0.06 % are to be used. The review revealed that for a sensor supply voltage of +/-15 V and a current of 2 A, sensor types with a measurement range from 12.5 A to 2000 A are available, with accuracies ranging from 509 ppm to 12 ppm. This range of sensor types is sufficient for the application of the cell monitor. This block has been revised to provide a supply current up to 2 A at +/-15 V.

On the input side, the existing DC-DC converters have been replaced with the TEN 60-2423WIN model to ensure a stable current of 2 A. The TEN 60-2423WIN generates a ripple of 125 mV at 250 kHz at the output. This ripple should be reduced using a Pi filter at the output to enhance the quality of the sensor power supply, as a ripple in the supply voltage can affect the measurement signal captured by the fluxgate current sensors. Since the measurement signals have a bandwidth of up to 25 kHz, the cutoff frequency f_c of the Pi filter should be set at 25 kHz. The ripple of 125 mV occurs with an output capacitance of 10 µF, so this value is chosen for *C1*. To keep the inductance for *L* low and thus reduce the overall size, a 100 µF capacitor is chosen for *C2*. With these values, the inductance calculation is performed by substituting and rearranging equation (8.19). This results in an inductance value of 0.144 µH.

$$f_c = \frac{1}{2\pi\sqrt{L(C_1+C_2)}} \tag{8.19}$$

f_c/Hz Cut-off frequency

L/H Inductor value

C_1, C_2/F Capacitors value

Before designing the simulation circuit, real components are selected for the calculated values to ensure that the corresponding models can be applied in the simulation. For *L*, a 150 nH inductor from TDK (TFM322512ALMAR15MTAA) is chosen. For the 10 µF capacitor, a Würth X7R ceramic capacitor (8885012214006) is selected, and finally, a Panasonic electrolytic capacitor (ECA1JFQ101) is used for the 100 µF capacitor. All component parameters are transferred into a simulation circuit, and an AC analysis is performed where a positive 15 V DC voltage is superimposed with an AC voltage of 125 mV amplitude. It is assumed that the simulation results can be applied to the negative output as well, i.e., -15 V DC voltage. See Figure 89.

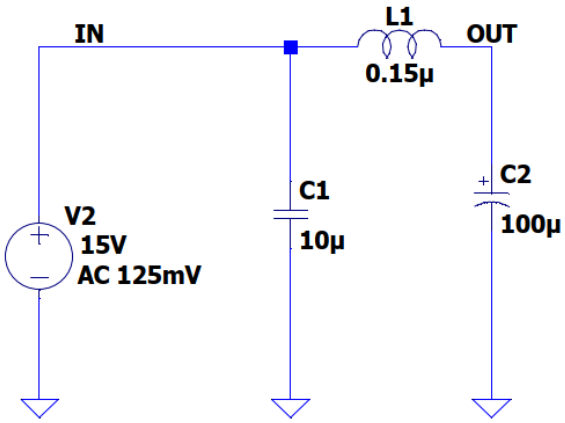


Figure 89: Simulation circuit of the output filter of the DC-DC converter, source: own illustration.

The simulation results (see Figure 90) show an attenuation of approximately -4.1 dB at 250 kHz, which corresponds to a voltage of around 78.3 mV, representing a reduction of 37.4 %.

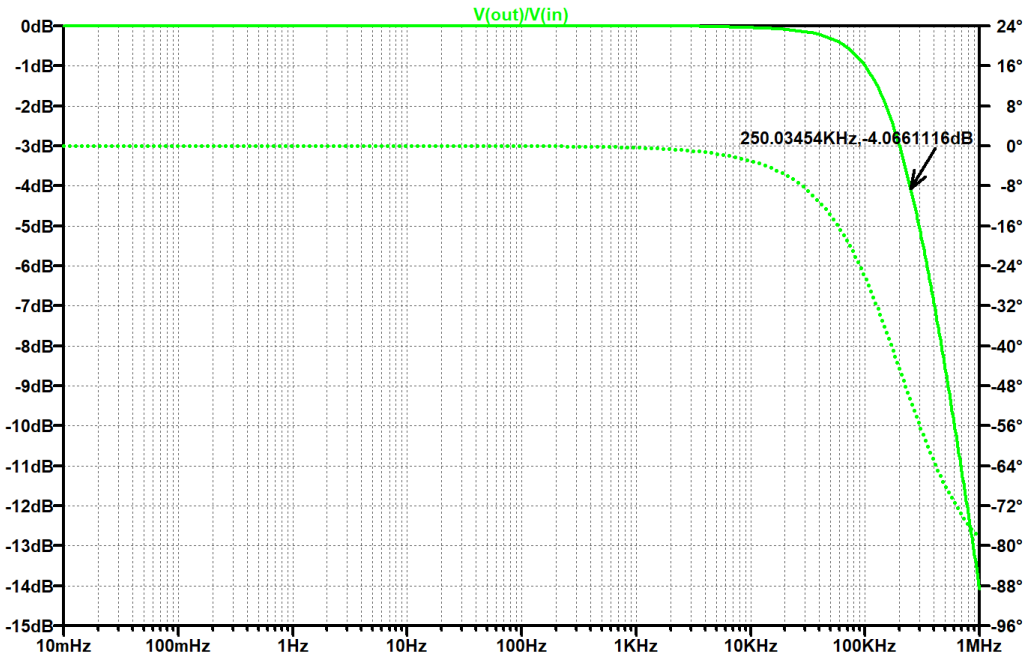


Figure 90: Amplitude and frequency response of the output filter, source: self-created.

Figure 91 shows the implemented circuit diagram. An output circuit was designed for the voltage outputs of the DC-DC converter to provide feedback on whether the DC-DC converter has been activated.

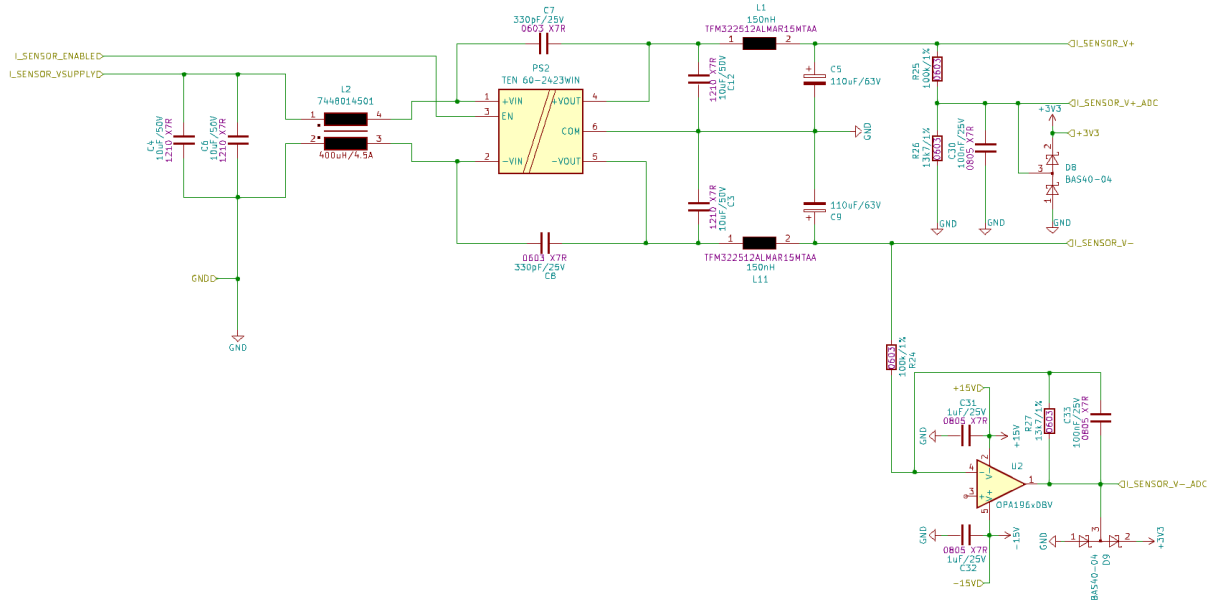


Figure 91: Circuit diagram of the DC-DC converter with output filter and feedback signal circuit, source: on illustration.

8.8 Microcontroller

The microcontroller features its own power supply which powers the respective circuit block. To enable programming of the microcontroller, a JTAG/SWD interface has been implemented. During circuit implementation, reference was made to a schematic of an evaluation board[60].

The pin assignment was created using STM32CubeMX. Through this software, pin configuration can be defined, such as specifying whether a pin functions as a GPIO or as the MOSI pin for SPI functionality. The file generated by STM32CubeMX can then be loaded into the IDE's editor, where all hardware presets, including code snippets, are provided.

Figure 92: Pin assignment of the STM32H747BIT6 generated in STM32CubeMX, source: own illustration.

Additionally, two temperature sensors have been integrated, positioned near the voltage measurement channel and current measurement channel, to capture ambient temperature and the temperature of the circuit board. This is aimed at determining the steady-state condition regarding heating to estimate to what extent temperature-related changes in components may still occur.

[60] Cf. STMicroelectronics (2017), Online-Source [1.2.2024].

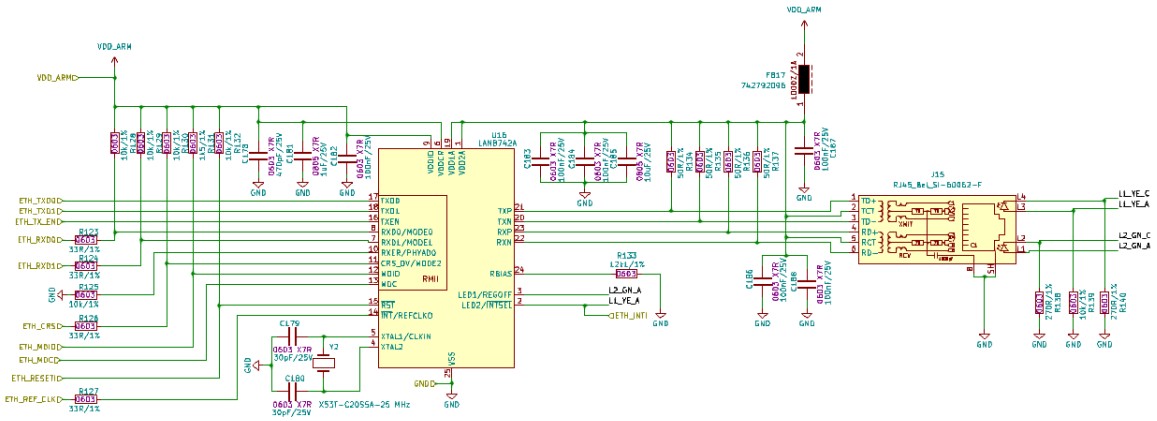


Figure 93: Circuitry configuration of the LAN8742A, source: own illustration.

Alongside the JTAG/SWD interface, an Ethernet interface has also been implemented. For this purpose, the IC LAN8742A has been connected to the microcontroller. The LAN8742A complies with IEEE802.3/802.3u and ISO 802-3/IEEE 802.3 standards. [61]

8.9 Voltage measurement channel

The voltage measurement channel comprises three circuit components. The measurement signal is introduced via the "Voltage Signal Connector" block. Considering the measurement range of up to 1000 V, alongside the provision for injecting a calibration signal to calibrate the voltage channel within the Internal Online Self-Calibration (IOSC) framework, a protective circuitry has been implemented. Following this, the voltage measurement signals undergo conditioning in the "High Voltage Attenuation and High Pass Filtering" block for further signal processing, before being digitized in the "Voltage Channel ADC" block. The entire signal path is illustrated in Figure 94.[62]

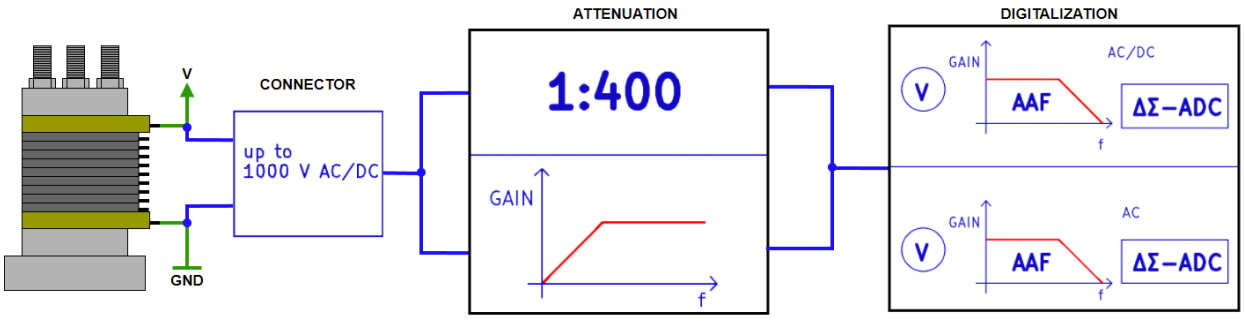


Figure 94: Signal path for the voltage measurement of the cell probe, source: own illustration.

[61] Cf. Microchip Technology Inc. LAN8742A (2015), Online-Source [14.3.2024] p. 1.

[62] Translation assistance by ChatGPT.

8.9.1 Voltage signal connector

A pluggable terminal block connector is employed as the interface. This allows for the connection of wires up to a size of 2,5 mm², eliminating the need for contacts to be attached to the wires. Positioned on the opposing side of the pluggable terminal block is integrated within the enclosure wall. Two wires from this opposing side are soldered to solder pads.

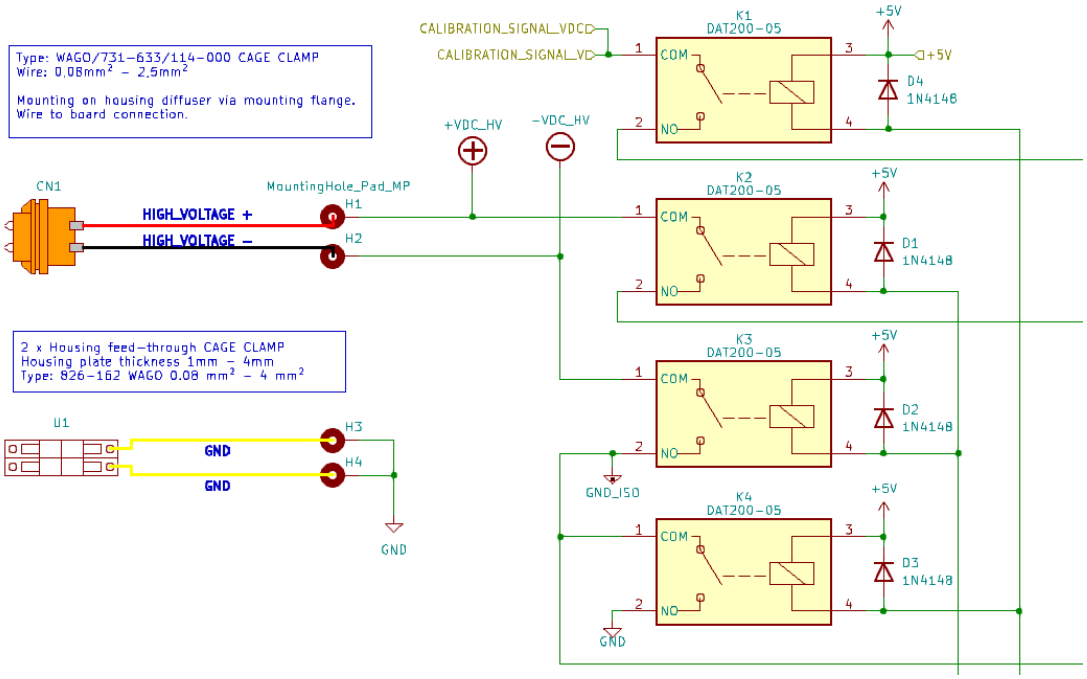


Figure 95: Connector interface of the voltage measurement input with mode switching circuitry, source: own illustration.

Four reed relays serve as switches between the calibration and measurement signals. The switching is controlled by the microcontroller and executed through a mutually locked transistor circuit.

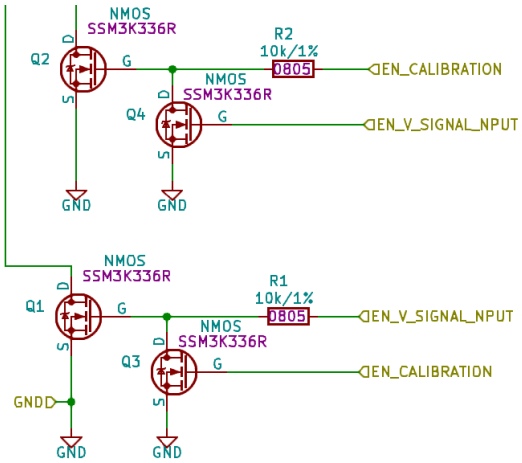


Figure 96: Locking circuit controlled by the microcontroller, source: own illustration.

The safety circuit comprises a 200 mA fuse, a reverse polarity protection implemented using a diode, and a current and power monitor IC of type ACS71020k. This IC measures the voltage across resistor R5 and the current flowing through it. At an output voltage of 1000 V, a current flow of approximately 125 µA is

established through the resistor, resulting in a voltage drop of around 1.25 V. If these values are exceeded, the connection to the voltage measurement signal is interrupted by controlling the microcontroller through the reed relays.

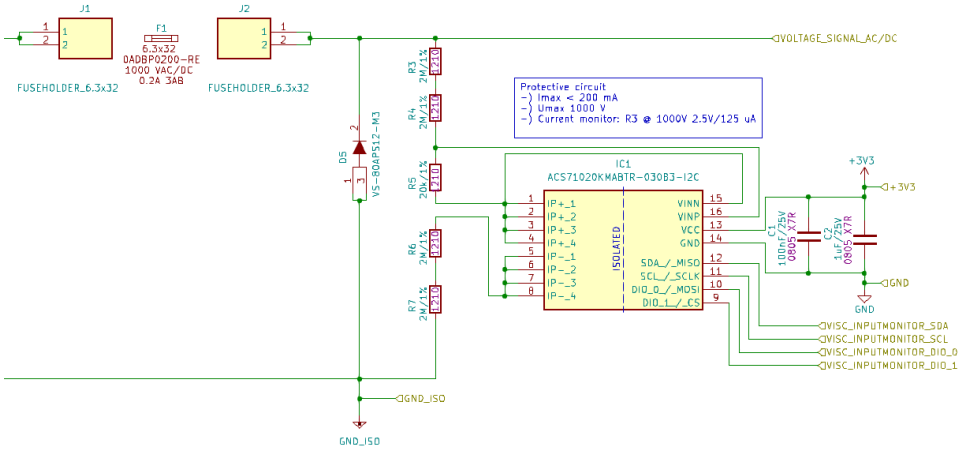


Figure 97: Structure of the safety circuit for the voltage measurement path, source: own illustration.

8.9.2 High voltage attenuation and high pass filtering

This circuit section is taken from the current schematic of the cell probe and has been adopted. The incoming measurement voltage from the "Voltage Signal Connector" block is processed in this block, in two channels: once as a mixed signal (U_{ACDC}) and once as a DC-decoupled AC signal. The mixed signal is attenuated by the high-voltage attenuation circuit to a voltage reduced by a factor of 400, resulting in an output voltage of 2.5 V for an input voltage of 1000 V.[63] There is the option to choose between two gain modes (1x and 10x). The simple gain mode is intended for voltages up to 100 V.

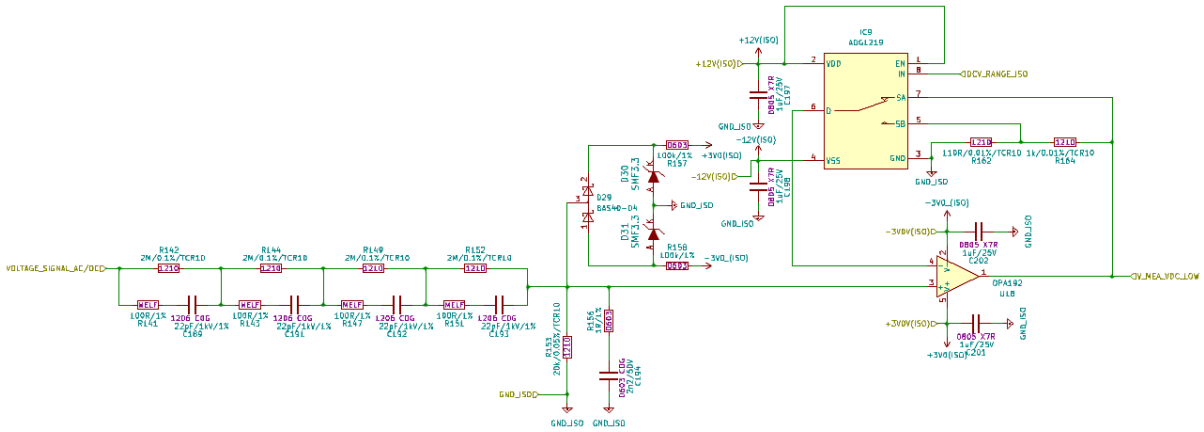


Figure 98: Circuit diagram of the high-voltage attenuator, source: own illustration.

The attenuation circuit was implemented as a frequency-compensated voltage divider, with particular emphasis on achieving a flat passband response up to 1 MHz. The output voltage was set to 2.5 V due to the availability of high-speed and high-impedance amplifiers that were installed after the voltage divider.

[63] Translation assistance by ChatGPT.

Additionally, it is worth mentioning that an ADC reference voltage of 2.5 V is a standard value for reference voltage sources. Resistors R142 to R152 act as voltage dividers at DC and low frequencies. Precision resistors with low temperature coefficients were chosen to avoid or acceptably minimize nonlinear effects caused by self-heating of the resistors. For higher frequency measurement signals, the capacitors act as a voltage divider. Capacitors of the C0G type were used to achieve high voltage resistance and temperature stability. Damping resistors R141 to R151 are used to reduce power losses of the capacitors.[64]

Due to the relatively small measurement voltages encountered in EIS measurements (4.2.3), a high-pass filter was additionally implemented to separate the AC measurement signal from the higher DC signal. This enables a better resolution of the voltage measurement signal. The cutoff frequency was designed to be 0.1 Hz, and the maximum allowable input voltage was set to +/-10 V. The high-pass filter was designed as a third-order Butterworth high-pass, which delivers 2.5 V at the output (1/4 of the input voltage) at full scale.

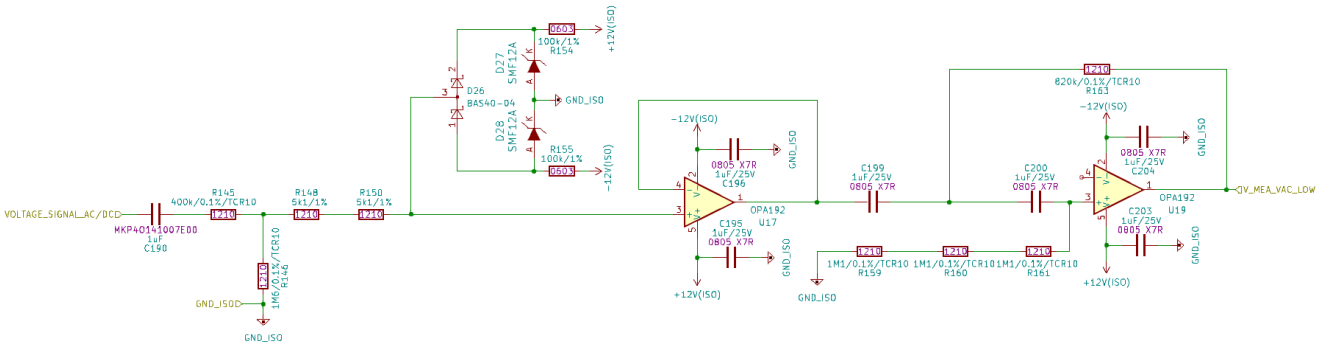


Figure 99: 0.1 Hz decoupled high-pass filter circuit, source: own illustration.

8.9.3 Voltage and channel ADC

The conditioned measurement signal, routed through the "High Voltage Attenuation and High Pass Filtering" block, is ultimately digitized in the "Voltage Channel ADC" block. To meet the required 16-bit resolution, a 24-bit delta-sigma converters of the type ADSL27L1L were selected. It can be assumed that phenomena such as noise decimate the resolution of 24 bits in order to still achieve the 16 bits, reserves are planned with regard to ADC resolution. The reference voltage of 2.5V is provided by a specialized voltage reference of the REF6025 type. An anti-aliasing filter (AAF) was implemented as a third-order Butterworth approximation low-pass filter in a multiple-feedback topology, with a cutoff frequency of 600 kHz. The sampling frequency of the delta-sigma ADC is 12.8 MHz. MFB filters offer a constant bandwidth range and low sensitivity to component tolerances. Additionally, they require a limited number of components, which improves noise performance. The diagram (Figure 100) depicts the ADC circuit,

[64] Cf. Grubmüller (2019) p. 33 – 39.

where the captured mixed signal is digitized. The channel digitizing the pure AC signal is identically configured.

For the filter design, an online filter design tool[65] provided by Texas Instruments was utilized. The following approach was taken: The sampling frequency of the ADC is 12,8 MHz, meaning that the clock frequency at which the ADC operates is 25.6 MHz, resulting in a Nyquist frequency of 6.4 MHz. The passband of the Anti-Aliasing Filter (AAF) is set at 25 kHz, as specified (5.2 p. 20) indicating that the useful signal extends up to that frequency. To achieve minimal gain ripple in the passband, a Butterworth approximation was employed. Since the attenuation of the signal begins before the cutoff frequency in a Butterworth filter, the cutoff frequency was set not at 25 kHz but at 60 kHz. The attenuation is adjusted to achieve -60 dB at 600 kHz. Given that the filter design is realized as a multiple feedback filter and implemented with operational amplifiers, where an additional amplification factor can be adjusted, a gain factor of 1 was chosen.

The circuit proposed by the filter design tool is depicted in Figure 100. It consists of a two-stage filter. The first stage comprises a first-order low-pass filter cascaded with a second-order low-pass filter.

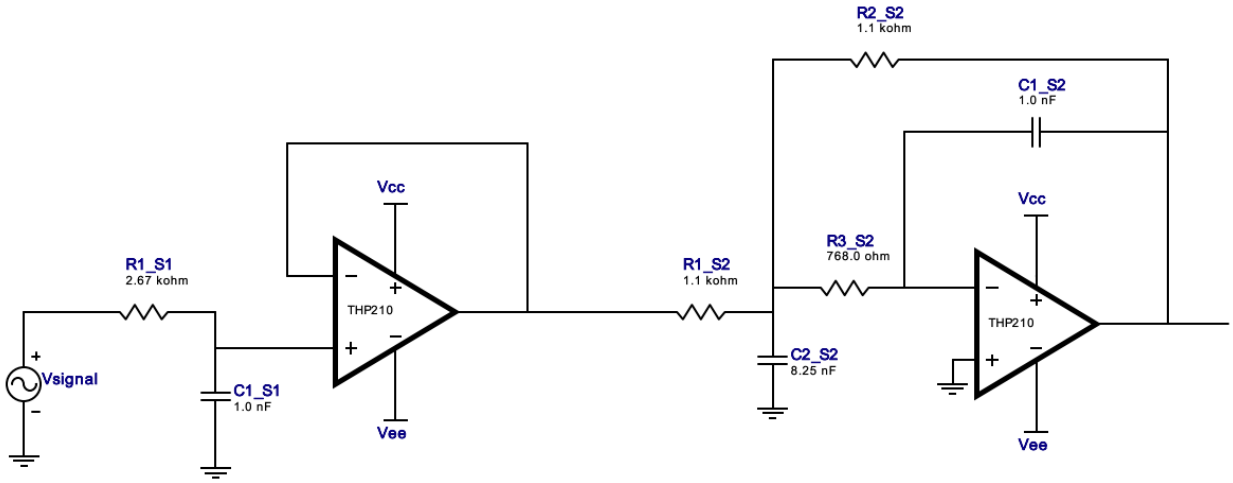


Figure 100: Cascaded Butterworth low-pass filter created by the filter design tool, source: own illustration.

The result (see Figure 101) depicts the amplitude and phase response of the filter. It meets the specifications regarding the -60 dB attenuation at 600 kHz and the cutoff frequency (-3 dB) at 60 kHz.

[65] Cf. Texas Instruments Incorporated (2024), Online-Source [1.5.2024].

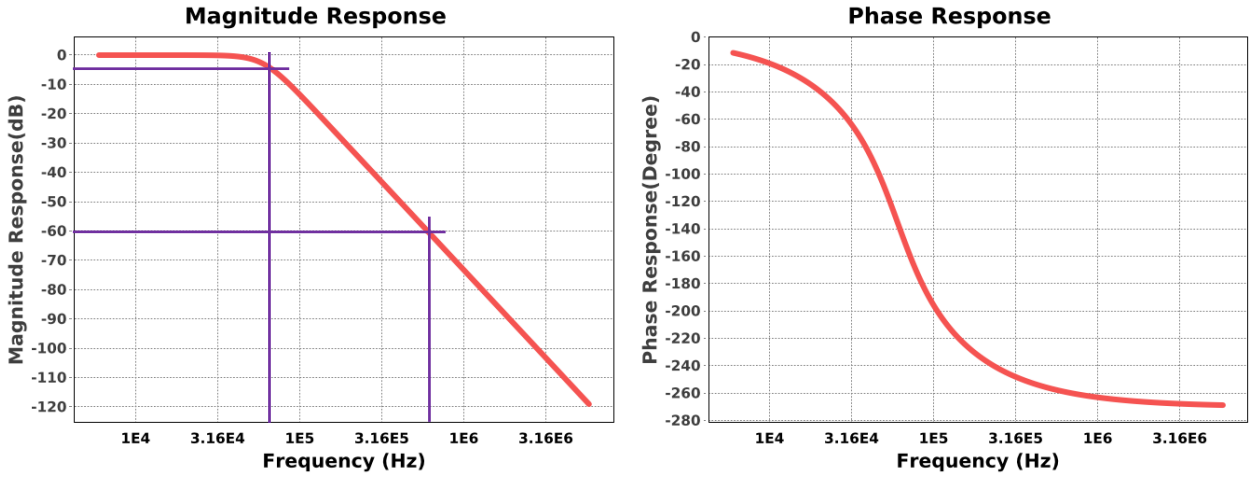


Figure 101:Amplitude and phase response of the 3rd order Butterworth low-pass filter generated by the filter design tool, source: self-created.

This circuit will not be adopted, because fully differential amplifiers will be used to implement the AAF, as the signal input of the ADC also requires a differential signal. However, the values of the resistors and capacitors will be adopted. To verify whether the adapted low-pass filter meets the specified requirements after adaptation, a simulation circuit will be created in LTspice.

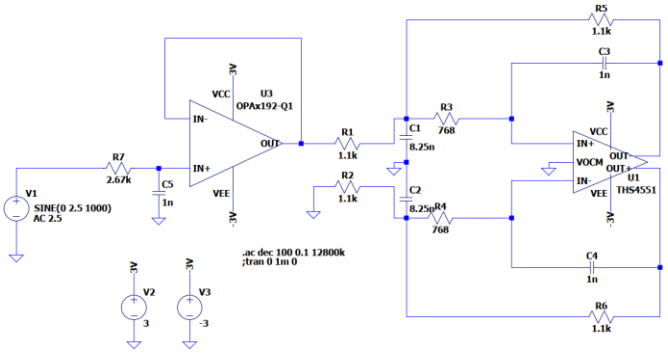


Figure 102: Adapted AAF as simulation model, source: own illustration.

An AC analysis was conducted from 0.1 Hz to 12.8 MHz. The amplitude value was set to 2.5 V, corresponding to the output provided by the "High Voltage Attenuation and High Pass Filtering" block. The output signal is differential, so the measurement point is set between OUT+ and OUT- (the position of the reference probe).

In section A of Figure 103, signal is attenuated by approximately 47 mdB from 0.1 Hz to 25 kHz. This attenuation of the measurement signal is acceptable and possible deviations can be corrected during calibration. No amplitude ripple is apparent in the frequency range of the measurement signal of the simulation results. The cutoff frequency (-3 dB) is at 60 kHz, as shown in Figure 103 B. At 600 kHz, there is a 60 dB attenuation (Figure 103 C). Although the attenuation is lower than the development target, an attenuation of 60 dB is sufficient for use on the cell probe. Point D in Figure 103 indicates a phase shift of up to -50 ° over a measurement signal span from 0.1 Hz to 25 kHz. All design requirements were met by the designed AAF. Therefore, it will be transferred to the schematic.

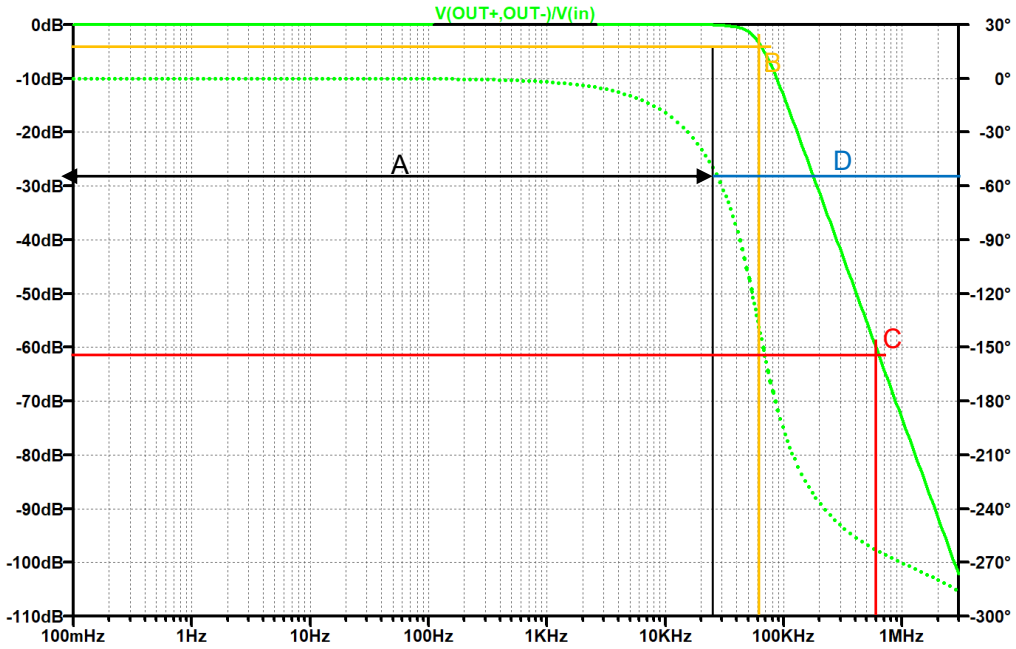


Figure 103: Amplitude and phase response of the simulation circuit, source: self-created.

Below Figure 104 is the circuit implementation of the AAF including the ADC and its associated reference voltage source. This circuit is utilized for both the processing of mixed signal data and the DC-decoupled AC signal, as well as for the current measurement channel.

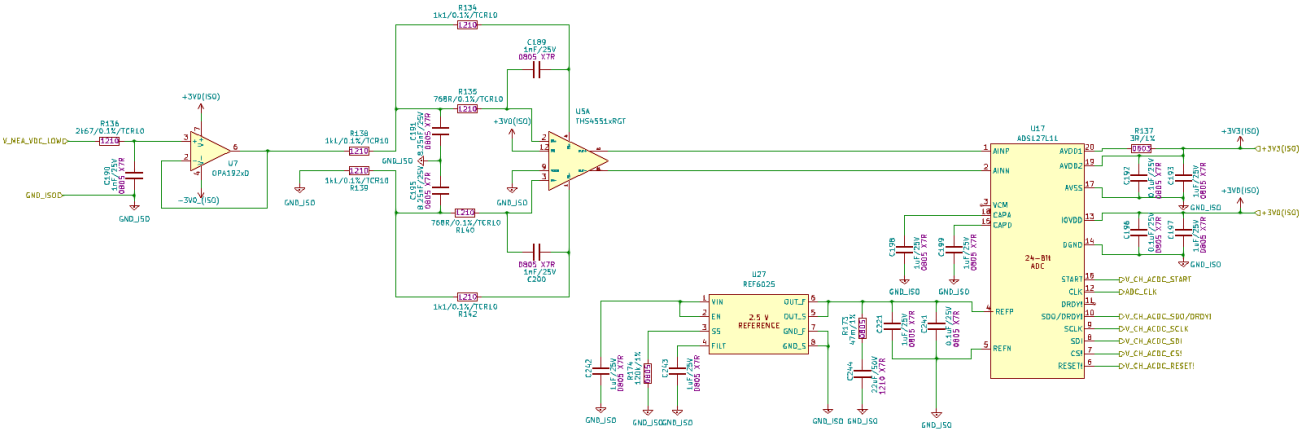


Figure 104: Final ADC circuit with implemented AAF, source: own illustration.

8.10 Current channel

The current measurement channel features five different measurement channels, enabling the connection of various Fluxgate current sensors. Channel 1 allows for voltage-supplying Fluxgate current sensors delivering +/-10 V to be evaluated. Channels 2 - 5 are designated for connecting current-supplying Fluxgate current sensors. Sensor currents ranging from +/-20 mA, +/-500 mA, ±1 A, and ultimately sensors providing a secondary current of +/-2 A can be processed. Each channel can only accommodate one sensor. The respective measurement signal is routed to the ADC via analog multiplexers (IC5 to IC7). Connectors J8 to J12 not only introduce the measurement signal but also provide sensor power (see Chapter 8.7). Between the connector and the analog multiplexer, each channel is equipped with an overvoltage protection circuit. Additionally, a circuit function has been implemented to identify which channel is plugged in.

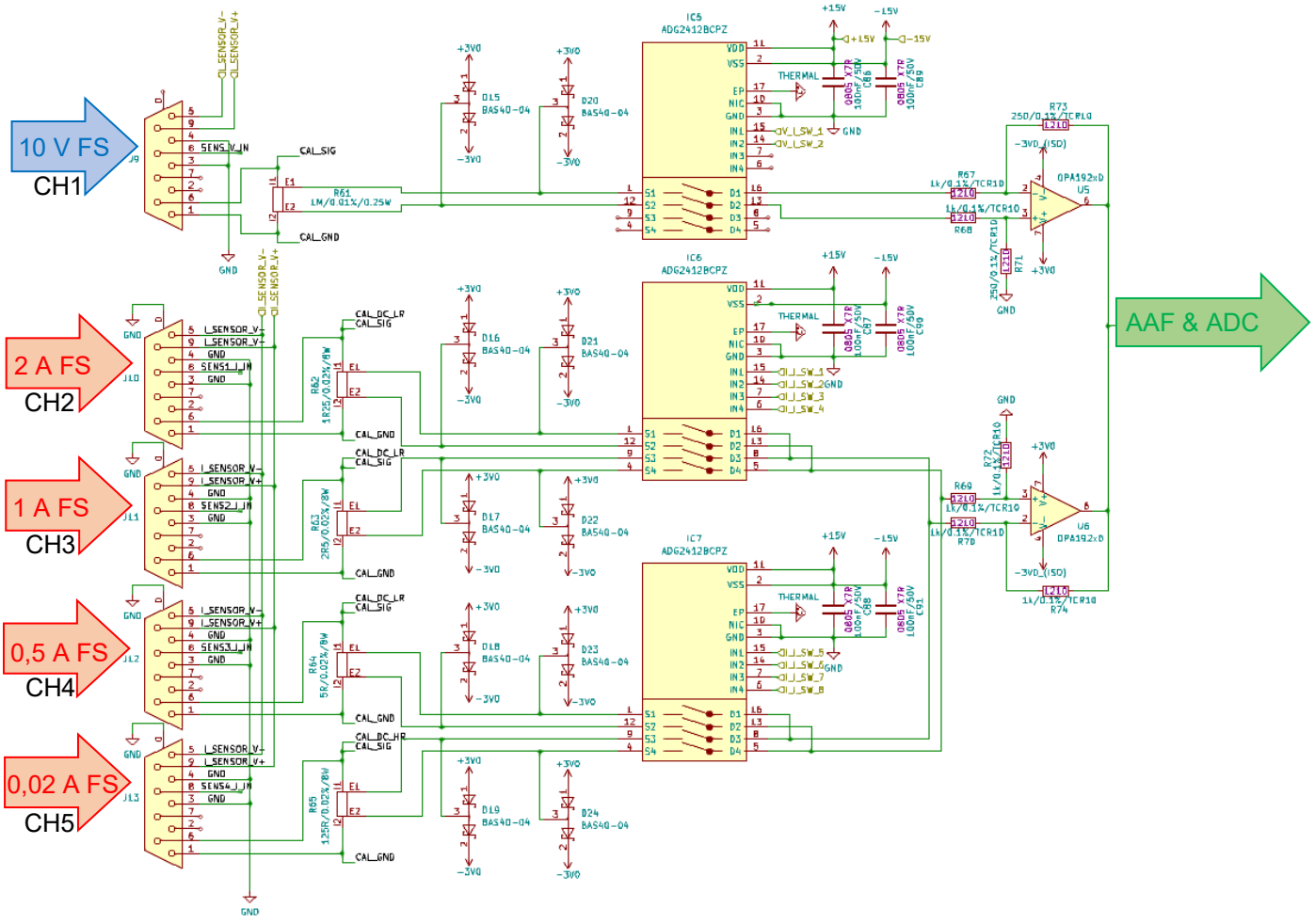


Figure 105: Input circuitry of the current measurement channel including the five sensor channels and analog multiplexed signal path, source: own illustration.

The channel detection is achieved by connecting the ground potential present at pins 4 and 3 of the Sub-D connector to pin 8 via a wire bridge on the sensor side.

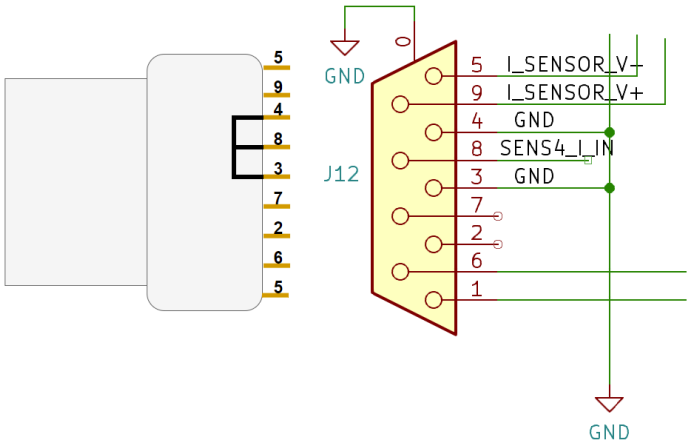


Figure 106: Wiring diagram illustrating the channel detection function, source: own illustration.

The pin 8 of each sensor channel connector is routed to a transistor circuit. Upon application of the ground potential, the respective transistor is activated, enabling a transition from 3.3 V to ground. This signal variation is subsequently assessed by the microcontroller. Consequently, the specific current measurement channel, along with its corresponding secondary signal range and sensor type, is identified. This information is then utilized to configure the analog multiplexer according to the requirements.

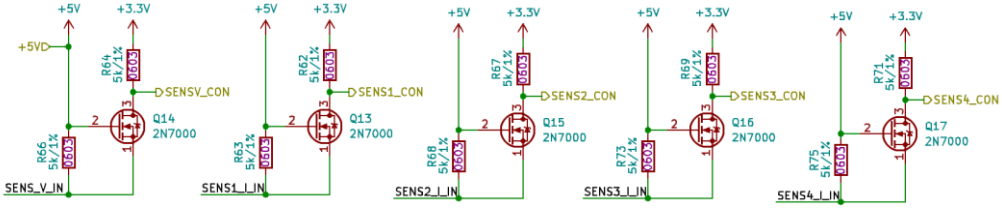


Figure 107: Channel detection evaluation unit serving as signal generator for the microcontroller, source: own illustration.

8.11 Measurement quality analysis

In this chapter, the measurement channels are verified and validated with respect to signal processing quality. To achieve this, four simulation models are developed:

1. The voltage measurement channel with single-stage amplification.
2. The voltage measurement channel with tenfold amplification.
3. The voltage measurement channel with DC decoupling.
4. The current measurement channel.

For each model, the frequency response is simulated taking into account component tolerances. In the second step, the impact of elevated ambient temperature is examined. Finally, a noise analysis of the measurement channels is conducted.

The procedure begins with simulating the circuit unaffected by temperature or component tolerances. These simulation results are subsequently referred to as the ideal circuit and its simulation values as ideal. The amplitude and phase are then measured at 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, and 25 kHz using the cursor function. Figure 108 and Figure 109 graphically illustrate the ideal amplitude and phase response of the voltage measurement channel with single-stage amplification. This process is repeated for the simulation results of the circuit under tolerance and temperature influences, with the cursor measurements representing the minimum and maximum values at the previously defined frequencies. Subsequently, the results are tabulated and calculated to determine how the values deviate from the ideal in both absolute and percentage terms. This approach yields reliable estimates of deviations, serving as a basis for subsequent calibration efforts.

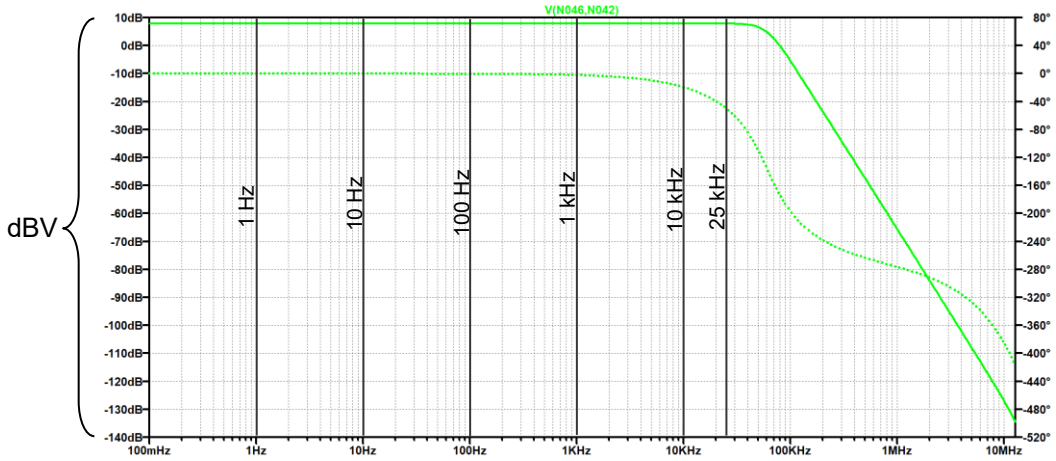


Figure 108: Amplitude and phase response of the voltage measurement channel with single-stage amplification, with marked measurement points (in **dBV**), source: self-created.

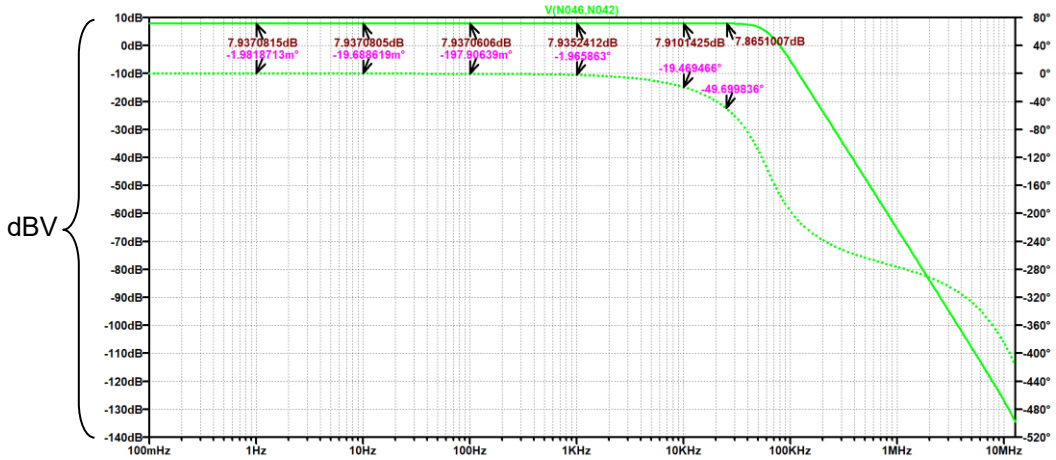


Figure 109: Amplitude and phase response of the voltage measurement channel with single-stage amplification, with annotated cursor measurements for amplitude and phase (in **dBV**), source: self-created.

For noise estimation, all components of the circuit contributing to signal noise are added to the simulation model. This includes, for example, the contact resistances of the analog multiplexer in the current measurement channel and the output noise of the linear voltage regulators supplying the operational amplifiers. LT-Spice provides the spectral noise density across the frequency range. The integrated function within LT Spice provides the RMS value of the noise, which is required for further analysis.

8.11.1 Voltage channel with single-stage amplification

The simulation model has been streamlined to focus on the most relevant components, with the circuit adjusted to suit the requirements of the applied simulation. At this point, the three analysis steps are shown explicitly using the “voltage channel with single-stage amplification” circuit block. For the other three circuit blocks, only the results are documented.

8.11.1.1 Influence of component tolerances

To evaluate the influence of component tolerances, a Monte Carlo simulation is being implemented. In this approach, the catalogue values of the components along with their tolerance values are embedded within the component model. Subsequently, the iterations are defined using the `.step` directive. Specifically, 20 steps regarding resistors and 20 steps regarding capacitors are to be conducted, resulting in a total of 400 iterations. An AC analysis is then executed to ascertain alterations in both amplitude and phase response concerning tolerances. The amplitude and phase response were measured between OUT- and OUT+ at the output of the AFF on the FDA U6. If not explicitly specified, the default ambient temperature in LTspice is 27°C. The simulation results are depicted below in Figure 110.

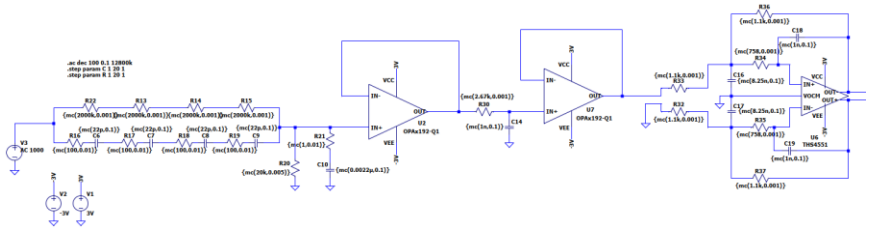


Figure 110: Simulation circuit for applying Monte Carlo simulation of the voltage channel with single-stage amplification, source: own illustration.

The amplitude gain change (G_E) and phase shift change ($\Delta\varphi_E$) are measured from the graphs and referenced to the ideal values (G_I and φ_I). Measurements are taken at 10 Hz, 100 Hz, 1 kHz, 10 kHz, and 25 kHz. The simulation results are compiled in tabular form under Table 4. Here, the values of the ideal amplitude and phase response (highlighted in violet) are compared with those derived from the two amplitude and phase responses exhibiting the greatest dispersion. Values from the amplitude and phase responses showing the lowest amplitude (highlighted in red) and the highest (highlighted in green) are also considered.

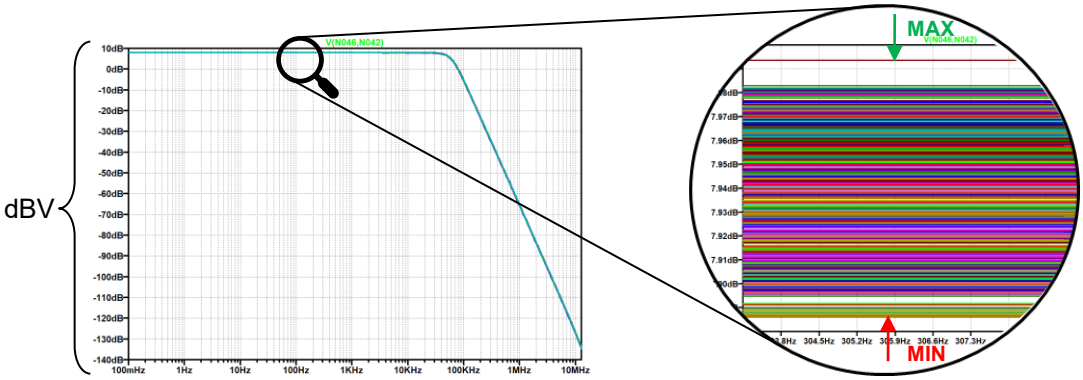


Figure 111: Definition of the maximum and minimum graphs from the simulation data based on the Monte Carlo results of the voltage channel with single-stage amplification, source: self-created.

	1 Hz		10 Hz		100 Hz	
G_I	0.922135188		0.922135063		0.922132575	
G_{EMAX}, G_{EMIN}	0.999205	0.985784375	0.999203375	0.985784238	0.999202638	0.985780688
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	7.06	-6.35	0.0565465	-0.0508066	0.0565605	-0.0508151
ΔG_{EMAX}, ΔG_{EMIN} / %	0.712	-0.640	0.712	-0.640	0.713	-0.640
φ_I / °	-0.001981873		-0.019688619		-0.19790639	
φ_{EMAX}, φ_{EMIN} / °	-0.0019454789	-0.0019738513	-0.019425172	-0.01970892	-0.19423605	-0.19706933
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	3.64E-05	8.02E-06	0.0003	-2.03E-05	0.004	0.001
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	-1.836	-0.405	-1.338	0.103	-1.855	-0.423
	1 kHz		10 kHz		25 kHz	
G_I	0.99190515		0.988767813		0.983137588	
G_{EMAX}, G_{EMIN}	0.999134188	0.985451988	0.9977066	0.98128095	0.991499213	0.9763709
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	7.229038	-6.6832	8.938787	-10.85411	8.361625	-15.76167
ΔG_{EMAX}, ΔG_{EMIN} / %	0.729	-0.651	0.904	-0.757	0.851	-0.688
φ_I / °	-1.966		-19.469		-49.7	
φ_{EMAX}, φ_{EMIN} / °	-1.9415454	-1.9660254	-19.394861	-19.195364	-49.754643	-49.106663
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	0.0243176	-0.0001624	0.074605	0.274102	-0.054807	0.593173
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	-1.237	0.008	-0.383	-1.408	0.110	-1.194

Table 4: Measurement results of the Monte Carlo analysis of the voltage channel with single-stage amplification, source: self-created.

At each measurement point, the maximum and minimum values of the amplitude and phase responses generated by the Monte Carlo analysis were documented. These values were then expressed as a percentage of the reference values G_I and φ_I. It is evident that the error in the amplitude response increases with frequency, while that of the phase response decreases.

8.11.1.2 Temperature dependency

To estimate the temperature dependency of the circuit, parameters for resistors were created considering their associated temperature coefficients. For capacitors, models based on real components were used, and the operational amplifiers also accounted for temperature variations.

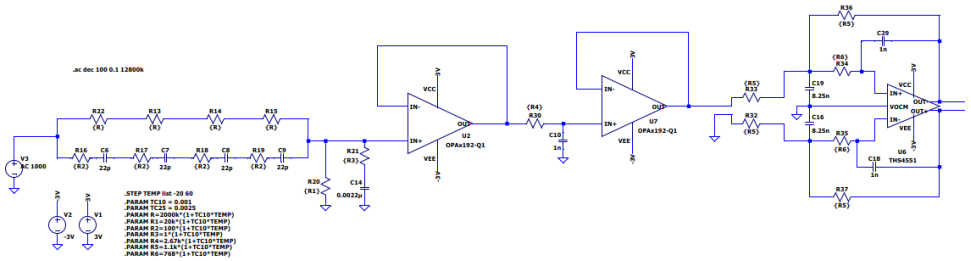


Figure 112: Simulation circuit for assessing the temperature dependency of the voltage channel with single-stage amplification, source: own illustration.

	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	25 kHz
$G_{-20°C}$	0.99213518	0.99213504	0.99213266	0.99191	0.98894394	0.98435605
$G_{+60°C}$	0.99213523	0.9921351	0.99213231	0.99187489	0.98881455	0.98247315
ΔG_T / x10^{-3}	-5E-05	-6.25E-05	3.5E-04	3.51125E-02	0.129388	1.8829
ΔG_T / %	-0.00000504	-0.00000630	0.00003528	0.00353989	0.01308340	0.19128241
$\varphi_{-20°C}$ / °	-0.001989256	-0.019924911	-0.19547949	-1.9578642	-19.352379	-49.207103
$\varphi_{+60°C}$ / °	-0.00214994	-0.02153897	-0.21131627	-2.115959	-20.928688	-53.506012
$\Delta\varphi_T$ / °	0.000160684	0.001614059	0.01583678	0.1580948	1.576309	4.298909
$\Delta\varphi_T$ / %	-8.07761334	-8.10070871	-8.10150466	-8.07486035	-8.14529831	-8.73635865

Table 5: Measurement results of a variable ambient temperature of the voltage channel with single-stage amplification, where the ambient temperature was first set to -20°C and then increased to 60°C, source: self-created.

Due to the low temperature coefficients of the components, the change in amplitude from an ambient temperature of -20 °C to +60 °C is very small. Even at a constant temperature, such as 60 °C, the amplitude exhibits similar behaviour across frequencies as it does at -20 °C. However, the phase shift from -20 °C to +60 °C is approximately 8 % smaller. Nevertheless, the 8 % phase shift remains relatively constant across frequencies.

8.11.1.3 Noise estimation

The simulation circuit was expanded to account for the noise of the +3,3 V and -3,3 V regulators by adding a noise voltage source in series with the actual voltage source. The noise behaviour of both the positive and negative voltage outputs was extracted from the datasheets of the LM27762DSSR. Both outputs exhibit an RMS noise of 22 μV_{RMS} at an ambient temperature of 25 °C and a bandwidth of 10 Hz

to 100 kHz.[66] Based on this, the spectral noise voltage density is calculated to integrate this value into the source parameters (see Equation (8.20)).

$$V_{Nf} = \frac{V_{RMS}}{\sqrt{f_{MAX} - f_{MIN}}} \quad (8.20)$$

V_{Nf}/VHz$^{-1/2}$ Spectral noise voltage density

V_{RMS}/V RMS noise

f_{MAX}/s^{-1} Maximum frequency

f_{MIN}/s^{-1} Minimum frequency

Thus, a spectral noise voltage density at 25 °C and a bandwidth of 99,99 kHz yields 69,6 nVHz$^{-1/2}$. This value was applied to both voltage sources supplying the operational amplifiers. (See Figure 113) The noise analysis was conducted at an ambient temperature of 60 °C, as noise levels increase with temperature, making 60 °C the worst-case scenario.

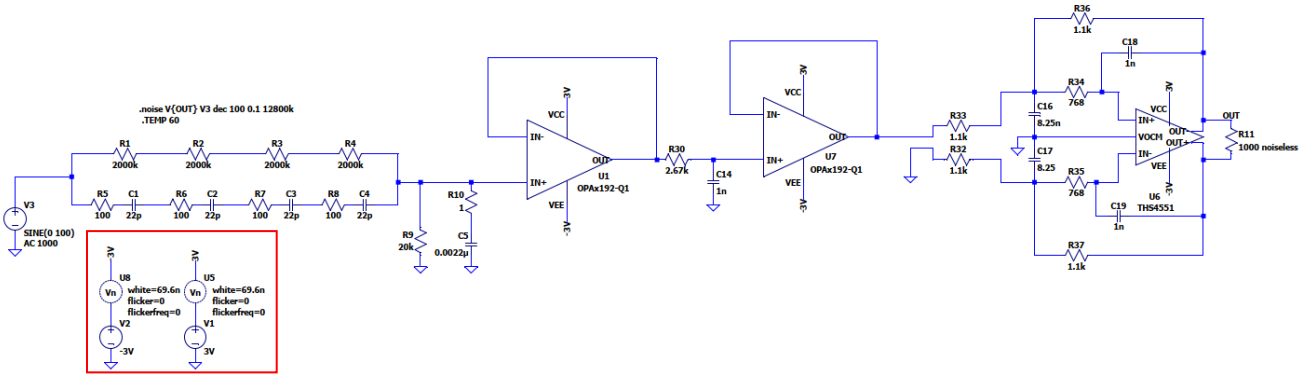


Figure 113: Simulation circuit for noise analysis to estimate the noise occurrence of the circuit block at an ambient temperature of 60°C, source: own illustration.

The voltage was measured at the differential output of the AAF, with a resistor connected between the outputs. This resistor does not affect the noise due to the "noiseless" input. Figure 114 illustrates the simulation results.

[66] Cf. Texas Instruments Incorporated (2016), Online-Source [2.1.2024] p. 5.

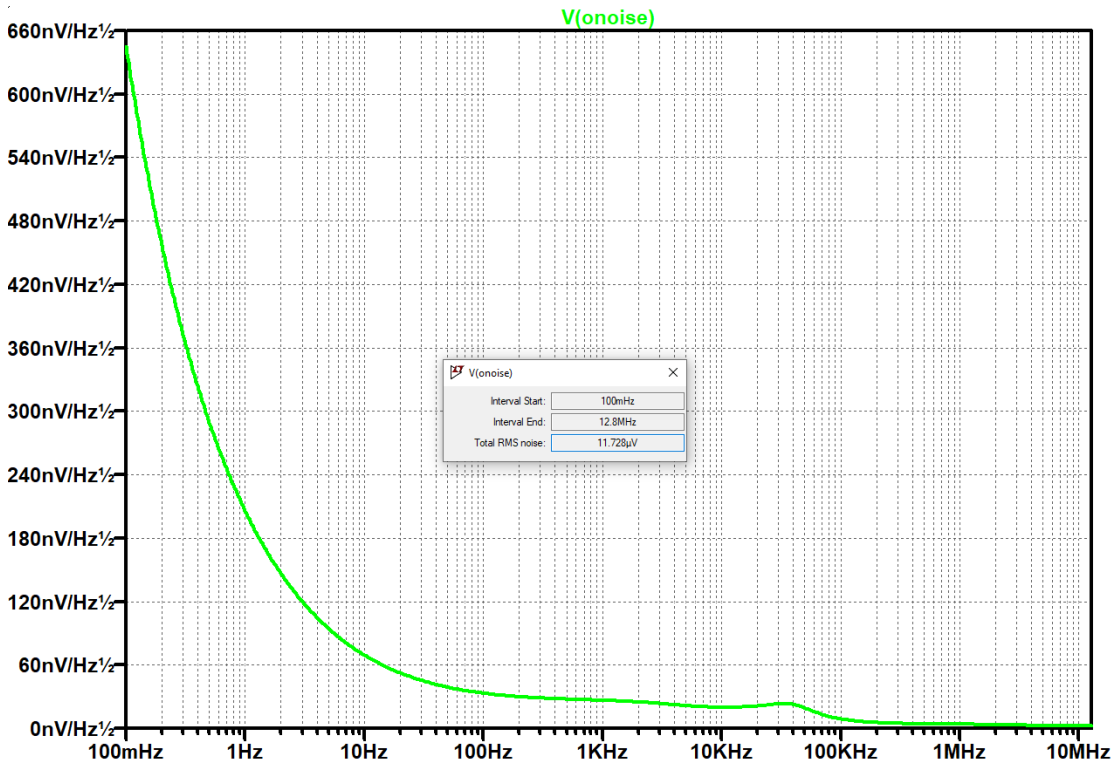


Figure 114: The simulation result as a noise spectrum, source: self-created.

The circuit adds an RMS noise of 11.728 µV at the output (*V(onoise)*). To calculate the signal-to-noise ratio, the amplitude values of the ideal circuit, the circuit affected by component tolerances, and the temperature dependency are used. The worst-case results of temperature dependency and tolerance are summarized to calculate the SNR values at the end. The values given in dB are converted from the peak values to $V_{SIGNALRMS}$, and then the SNR is calculated at an ambient temperature of 60°C. LTspice calculates the integral of the squared values of the curve over the frequency and then takes the square root to determine the RMS noise value.

The evaluation was implemented using a spreadsheet tool, following these calculation steps:

1. Initially, the amplitude values from the Monte Carlo analysis and the temperature analysis were transferred to columns "V_{OUTMC}" and "$V_{OUTTEMP}$," respectively.
2. Subsequently, the difference between the ideal output signal (first row of column "V_{OUT}") and the temperature-affected signal (column "$V_{OUTTEMP}$") was calculated and added to the results of the Monte Carlo analysis (column "V_{OUTMC}").
3. In column "V_{OUTMC}," the values for the lowest and highest amplitudes at the 25 kHz point were entered as maximum and minimum values. These steps assume that the change in ambient temperature shifts the operating point of the ideal amplitude response. In other words, a Monte Carlo analysis of the circuit would be performed at -20°C and 60 °C instead of 25 °C to consider both influences in the SNR calculation.

The SNR is calculated according to Equation (8.21), where V_{SRMS} represents the RMS value of the signal, and V_{NRMS} represents the RMS value of the noise.

$$SNR = 20 \cdot \log \frac{V_{SRMS}}{V_{NRMS}} \tag{8.21}$$

V_{SRMS}/V RMS value of the signal voltage

V_{NRMS}/V RMS value of the noise

SNR/dB Signal noise ratio

	V_{OUTMC} / dB	$V_{OUTTEMP}$ / dB	V_{OUT} / dB	V_{OUT} / V	V_{OUTRMS} / µV	SNR / dB
A_I	-	-	7.8651007	2.473176066	1.748799567	103.470
$A_{Emax60°C}$	7.9319937	7.8597852	7.9373092	2.493822047	1.76339848	103.543
$A_{Emin-20°C}$	7.8109672	7.8748484	7.8012195	2.45505358	1.73598504	103.406

Table 6: SNR calculation under the influence of component tolerances and considering an ambient temperature of -20 °C and 60 °C, when introducing a 25 kHz signal, for the voltage channel with single-stage amplification, source: self-created.

The results are depicted in Table 6. An SNR of approximately 103 dB is achieved, meeting the specification. Furthermore, this analysis will be carried out for each circuit block using the same procedure.

8.11.2 Voltage channel with tenfold amplification

The Monte Carlo results, depicted in Table 7, illustrate the influence of component tolerances. The 'Voltage Channel with Tenfold Amplification' block generally behaves similarly to single-stage amplification. The amplitude values across frequencies are slightly higher on average. In terms of temperature variation, it behaves similarly stable to single-stage amplification.

	1 Hz		10 Hz		100 Hz	
G_I	1.001954325		1.001952788		1.0019503	
G_{EMAX}, G_{EMIN}	1.023272388	0.98161085	1.02327085	0.981609363	1.023269963	0.981611825
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	21.318063	-20.343475	21.318063	-20.34346	21.319662	-20.33848
ΔG_{EMAX}, ΔG_{EMIN} / %	2.128	-2.030	2.128	-2.030	2.128	-2.030
φ_I / °	-0.002085761		-0.020456634		-0.20436255	
φ_{EMAX}, φ_{EMIN} / °	-0.002047329	-0.001980566	-0.0200691	-0.0194073	-0.2004879	-0.1938773
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	3.84316E-05	0.000105194	0.00038754	0.00104937	0.00387461	0.01048521
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	-1.843	-5.043	-1.894	-5.130	-1.896	-5.131
	1 kHz		10 kHz		25 kHz	
G_I	1.001725863		0.9988576		0.994297163	
G_{EMAX}, G_{EMIN}	1.023193438	0.98184745	1.021842588	0.984358838	1.0168316	0.981063288
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	21.467575	-20.106875	22.984987	-17.59395	22.534437	-20.88701
ΔG_{EMAX}, ΔG_{EMIN} / %	2.143	-2.007	2.301	-1.761	2.266	-2.101
φ_I / °	-2.0404547		-20.118556		-51.813045	
φ_{EMAX}, φ_{EMIN} / °	-2.0039003	-1.9423126	-20.001231	-19.910854	-51.53069	-51.505242
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	0.0365544	0.0981421	0.117325	0.207702	0.282355	0.307803
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	-1.791	-4.810	-0.583	-1.032	-0.545	-0.594

Table 7: Measurement results of the Monte Carlo analysis of the voltage channel with tenfold amplification, source: self-created.

	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	25 kHz
$G_{-20°C}$	1.00195421	1.00195265	1.00195025	1.00173415	0.99888861	0.99470364
$G_{+60°C}$	1.00195466	1.0019532	1.00195041	1.00170024	0.99876516	0.99286028
ΔG_T / x10^{-3}	-4.5E-04	-5.5E-04	-1.625E-04	3.39125E-02	0.12345	1.843363
ΔG_T / %	-0.00004491	-0.00005489	-0.00001622	0.00338538	0.01235874	0.18531776
$\varphi_{-20°C}$ / °	-0.002047737	-0.020068573	-0.2004782	-2.0017876	-19.734926	-50.759747
$\varphi_{+60°C}$ / °	-0.002200093	-0.021543974	-0.21602452	-2.1565073	-21.271808	-55.00479
$\Delta\varphi_T$ / °	0.000152356	0.001475401	0.01554632	0.1547197	1.536882	4.245043
$\Delta\varphi_T$ / %	-7.44019410	-7.35179826	-7.75461871	-7.72907675	-7.78762484	-8.36301056

Table 8: Measurement results of a variable ambient temperature of the voltage channel with tenfold amplification, where the ambient temperature was first set to -20°C and then increased to 60°C, source: self-created.

The higher amplification results in slightly higher noise, leading to a slight degradation in the SNR. However, the specification is still met. The noise estimation yields an effective noise level of 14.394 μV_{RMS}.

	V_{OUTMC} / dB	$V_{OUTTEMP}$ / dB	V_{OUT} / dB	V_{OUT} / V	V_{OUTRMS} / µV	SNR / dB
A_I	-	-	7.9543773	2.498727319	1.766867031	101.780
$A_{Emax60°C}$	8.1346528	7.9428822	8.1461479	2.554508752	1.806310461	101.972
$A_{Emin-20°C}$	7.8485063	7.9576291	7.8452545	2.46753161	1.747773186	101.671325

Table 9: SNR calculation under the influence of component tolerances and considering an ambient temperature of -20 °C and 60 °C, when introducing a 25 kHz signal, for the voltage channel with tenfold amplification, source: self-created.

8.11.3 Voltage channel with DC decoupling

The AC decoupling high-pass filter, in conjunction with the AAF, forms a bandpass. This allows for the consideration of low frequencies and the assessment of how component variations affect the high-pass filter. The attenuation of approximately 50 dB per decade of the high-pass filter is sufficiently high.

	0.001 Hz		0.01 Hz		0.1 Hz	
G_I	-13.9277025		-6.427361375		0.658172538	
G_{EMAX}, G_{EMIN}	-13.92696875	-13.92806875	-6.42662138	-6.42771725	0.660037575	0.657591675
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	7.3375	-0.36625	0.74	-0.35588	1.865038	-0.58086
ΔG_{EMAX}, ΔG_{EMIN} / %	-0.005	0.003	-0.012	0.006	0.283	-0.088
φ_I / °	88.833565		78.312874		-48.943056	
φ_{EMAX}, φ_{EMIN} / °	88.834393	88.833579	78.321148	78.312932	-48.872497	-48.988952
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	0.000828	1.4E-05	0.008274	5.8E-05	0.070559	-0.045896
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	0.001	0.000	0.011	0.000	-0.144	0.094
	1 Hz		10 Hz		100 Hz	
G_I	0.994573588		0.994827413		0.9948291	
G_{EMAX}, G_{EMIN}	0.997124425	0.993522125	0.997381888	0.99378235	0.997383713	0.993783675
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	2.550837	-1.051462	2.554475	-1.04506	2.554613	-1.04543
ΔG_{EMAX}, ΔG_{EMIN} / %	0.256	-0.106	0.257	-0.105	0.257	-0.105
φ_I / °	-168.76063		-178.90388		-180.15272	
φ_{EMAX}, φ_{EMIN} / °	-168.75424	-168.76257	-178.90299	-178.9054	-180.15008	-180.16618
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	0.00639	-0.00194	0.00089	-0.00152	0.00264	-0.01346
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	-0.004	0.001	0.000	0.001	-0.001	0.007
	1 kHz		10 kHz		25 kHz	
G_I	0.994741638		0.986057313		0.939113338	
G_{EMAX}, G_{EMIN}	0.997303238	0.993651163	0.989230088	0.9808406	0.9431241	0.918928125
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	2.5616	-1.090475	3.172775	-5.21671	4.010762	-20.18521
ΔG_{EMAX}, ΔG_{EMIN} / %	0.258	-0.110	0.322	-0.529	0.427	-2.149
φ_I / °	-182.63867		-206.54716		-247.58942	
φ_{EMAX}, φ_{EMIN} / °	-182.61287	-182.77302	-206.30462	-207.834	-247.11217	-250.41136
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	0.0258	-0.13435	0.24254	-1.28684	0.47725	-2.82194
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	-0.014	0.074	-0.117	0.623	-0.193	1.140

Table 10: Extended measurement results of the Monte Carlo analysis of the voltage channel with DC decoupling amplification, source: self-created.

The effects of variable ambient temperature are depicted in Table 11.

	0.001 Hz	0.01 Hz	0.1 Hz	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	25 kHz
$G_{-20C°}$	-13.9935063	-6.49317888	0.62723729	0.99460156	0.99482766	0.99482895	0.99473054	0.98496916	0.93170893
$G_{+60C°}$	-13.7552363	-6.23752663	0.73639998	0.99456318	0.99482739	0.99482916	0.99474519	0.98640288	0.94142749
ΔG_T / x10^{-3}	-238.27	-255.65225	-109.162688	3.83875E-02	2.75E-04	-2.125E-04	-1.465E-02	-1.43371	-9.71856
ΔG_T / %	1.70271836	3.93724330	-17.40373056	0.00385959	0.00002764	-0.00002136	-0.00147276	-0.14555913	-1.04308999
φ_{-20C} / °	88.856895	78.547519	-46.046818	-169.3988	-178.96901	-180.17486	-182.7971	-208.13494	-251.78294
$\varphi_{+60C°}$ / °	88.770079	77.608593	-57.212366	-168.53047	-178.88045	-180.14517	-182.58584	-206.01817	-246.19871
$\Delta\varphi_T$ / °	0.086816	0.938926	11.165548	-0.86833	-0.08856	-0.02969	-0.21126	-2.11677	-5.58423
$\Delta\varphi_T$ / %	0.09770317	1.19536048	-24.24825099	0.51259513	0.04948343	0.01647844	0.11557076	1.01701809	2.21787465

Table 11: Measurement results of a variable ambient temperature of the voltage channel with DC decoupling, where the ambient temperature was first set to -20 °C and then increased to 60 °C, source: self-created.

In the noise analysis, the frequency range considered was extended to 1 mHz. Additionally, operational amplifiers are powered by a ±12 V voltage regulator, whose 100 µVrms[67] noise was accounted for using noise voltage sources analogous to the ±3 V regulators. This results in a spectral voltage noise density of 316.2 nVHz$^{-1/2}$. As a result, the circuit segment is subjected to a noise level of 13.281 μV_{RMS}.

	V_{OUTMC} / dB	$V_{OUTTEMP}$ / dB	V_{OUT} / dB	V_{OUT} / V	V_{OUTRMS} / µV	SNR / dB
A_I	-	-	7.5129067	2.374900041	1.679307924	102.038
$A_{Emax60°C}$	7.5449928	7.5314199	7.5264796	2.378614051	1.681934125	102.056
$A_{Emin-20°C}$	7.351425	7.4536714	7.4106603	2.34710768	1.644866259	102.438

Table 12: SNR calculation under the influence of component tolerances and considering an ambient temperature of -20 °C and 60 °C, when introducing a 25 kHz signal, for the voltage channel with DC decoupling, source: self-created.

[67] Cf. ANALOG DEVICE, INC: LTC3260 (2021), Online-Source [23.3.2024] p. 3.

8.11.4 Current channel

In the case of the current channel, the channel for the voltage-supplying fluxgate current sensors was considered since the input impedance is highest here. The results of the Monte Carlo analysis are summarized in Table 13. The results of component variations under temperature influence can be found in Table 14. The results of the noise analysis are in Table 15.

	1 Hz		10 Hz		100 Hz	
G_I	0.979869225		0.979869113		0.9798687	
G_{EMAX}, G_{EMIN}	0.98714065	0.982333075	0.987140525	0.982332963	0.98713945	0.982333325
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	7.271425	2.46385	7.271413	2.46385	7.27075	2.464625
ΔG_{EMAX}, ΔG_{EMIN} / %	0.742	0.251	0.742	0.251	0.742	0.252
φ_I / °	-0.002401415		-0.023984546		-0.23983074	
φ_{EMAX}, φ_{EMIN} / °	-0.002487612	-0.002247081	-0.0248465	-0.0224412	-0.2484501	-0.2243976
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	-8.61965E-05	0.000154334	-0.00086195	0.00154333	-0.0086194	0.01543316
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	3.589	-6.427	3.594	-6.435	3.594	-6.435
	1 kHz		10 kHz		25 kHz	
G_I	0.979828775		0.97584885		0.95249835	
G_{EMAX}, G_{EMIN}	0.98703085	0.982369463	0.985228488	0.976668275	0.98320055	0.929851038
ΔG_{EMAX}, ΔG_{EMIN} / x10^{-3}	7.202075	2.500238	5.359375	0.819425	3.33185	-22.64731
ΔG_{EMAX}, ΔG_{EMIN} / %	0.005	0.255	0.549	0.084	0.35	-2.378
φ_I / °	-2.3983782		-24.059061		-61.663279	
φ_{EMAX}, φ_{EMIN} / °	-2.4844678	-2.2441783	-24.822716	-22.635445	-62.647841	-58.998644
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / °	-0.0860896	0.1541999	-0.763655	1.423616	-0.984562	2.664635
$\Delta\varphi_{EMAX}$, $\Delta\varphi_{EMIN}$ / %	3.589	-6.429	3.174	-5.917	1.597	-4.321

Table 13: Measurement results of the Monte Carlo analysis of the current channel, source: self-created.

	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	25 kHz
$G_{-20C°}$	0.97986923	0.97986911	0.97986866	0.97982374	0.9753442	0.94831309
$G_{+60C°}$	0.97986926	0.97986915	0.97986876	0.97983046	0.9760105	0.95377314
ΔG_T / x10^{-3}	-3.75E-05	-3.75E-05	-1E-04	-6.725E-03	-0.6663	-5.46005
ΔG_T / %	-0.00000383	-0.00000383	-0.00001021	-0.00068635	-0.06831434	-0.57576449
φ_{-20C} / °	-0.00254428	-0.02541472	-0.25413325	-2.5414171	-25.504152	-65.600515
$\varphi_{+60C°}$ / °	-0.002353799	-0.023507837	-0.23506337	-2.3507002	-23.577777	-60.374347
$\Delta\varphi_T$ / °	-0.000190481	-0.001906883	-0.01906988	-0.1907169	-1.926375	-5.226168
$\Delta\varphi_T$ / %	7.48663551	7.50306515	7.50389018	7.50435259	7.55318193	7.96665697

Table 14: Measurement results of a variable ambient temperature of the current channel, where the ambient temperature was first set to -20 °C and then increased to 60 °C, source: self-created.

	V_{OUTMC} / dB	$V_{OUTTEMP}$ / dB	V_{OUT} / dB	V_{OUT} / V	V_{OUTRMS} / µV	SNR / dB
A_I	-	-	7.6199868	2.404359146	1.700138657	102.647
$A_{Emax60°C}$	7.4388083	7.6301851	7.42861	2.351963079	1.663089043	102.456
$A_{Emin-20°C}$	7.8656044	7.5865047	7.8990865	2.48287197	1.746848765	102.9263

Table 15: SNR calculation under the influence of component tolerances and considering an ambient temperature of -20 °C and 60 °C, when introducing a 25 kHz signal, for the current channel, source: self-created.

8.12 Configuration of the ADC

The following chapter describes the design decisions and configurations regarding the ADCs.

8.12.1 Clock source

A multiple-clock-buffer topology is employed to operate the ADCs in high-speed mode at 25.6 MHz. [68] This means that each of the three ADCs is supplied with its own clock source. The reason for this is that the voltage measurement channels are galvanically isolated from the rest of the electronics, including the current channels. Opting for a single clock source would inevitably compromise the isolation.

Additionally, in the PCB layout process, attention must be paid to ensuring that the traces from the clock source to the ADCs have the same geometrical and "electrical length". By electrical length, it is meant that traces, in combination with the parasitic capacitances and inductances of the PCB substrate, along with the ohmic losses through the copper, can cause differences in propagation delays, thereby affecting the synchronicity of the measurement channels.

Not only does the physical design play a role here, but also the quality of the clock source. Two parameters play a crucial role in this regard: clock jitter and channel-to-channel output skew. Clock jitter refers to fluctuations in the period duration of the clock signal, while input skew describes delays between the outputs of different clock sources when they are activated simultaneously. These parameters are important considerations in selecting the clock source and should be kept as minimal as possible. Output skew affects the synchronicity of signal processing. Clock jitter directly impacts the maximum achievable SNR of the ADC. (see Equation (8.22)) [69]

$$SNR_j = 20 \cdot \log \frac{2 \cdot \pi \cdot f_{in} \cdot t_j}{\sqrt{OSR}} \quad (8.22)$$

SNR_j/dB Theoretical SNR limit due to jitter

f_{in}/s^{-1} Input signal frequency

t_j/s-rms Clock jitter

OSR Oversampling ratio

[68] Cf. Texas Instruments Incorporated (2022), Online-Source [31.9.2023] p. 27.

[69] Cf. Texas Instruments Incorporated (2021), Online-Source [20.3.2024]. p. 3.

The I²C-controllable Si5338C is chosen as the clock source, which is already in use in the current version of the cell probe. This 4-channel clock source operates in GbE mode and operates within a temperature range of -40 °C to 85 °C, with an input clock of 25 MHz generated by a crystal oscillator, producing an output clock signal with a **maximum** jitter of 1 ps[70]. Theoretically, with an OSR of 32 and a signal frequency of 25 kHz, this setup **can** achieve an SNR greater than 145 dB (see Figure 115). Due to the low jitter of the clock source, the achieved SNR of the AAF is **not reduced**.

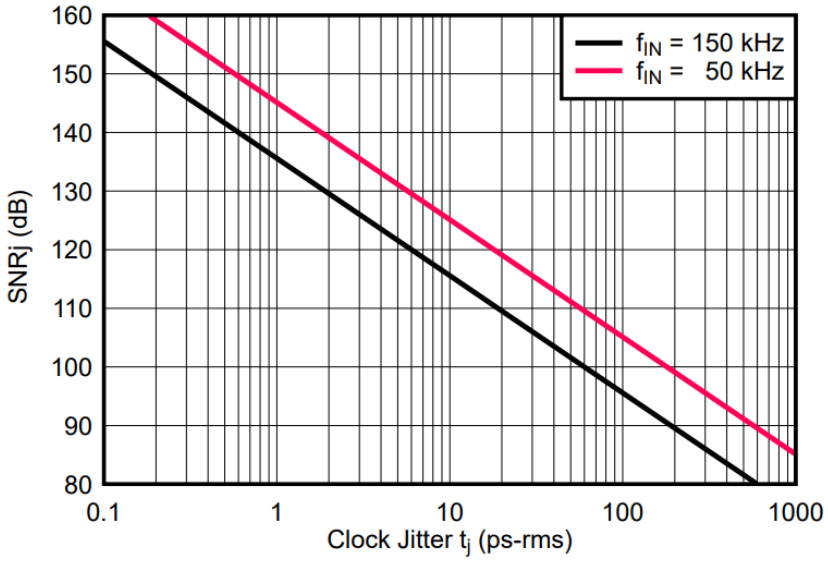


Figure 115: Signal-to-Noise Ratio Affected by Jitter, source: Texas Instruments Incorporated (2021), Online-Source [20.3.2024] p. 3.

Since the voltage measurement channel is galvanically isolated from the rest of the cell probe circuitry, the clock source for the ADC in the voltage measurement channel must also be isolated. This issue was resolved by using two separate clock sources. One clock source supplies, the ADC of the current measurement channel, which is connected to the second clock source via an interface IC that provides galvanic isolation. To prevent jitter between the two clock sources, they must be synchronized via the I2C interface.

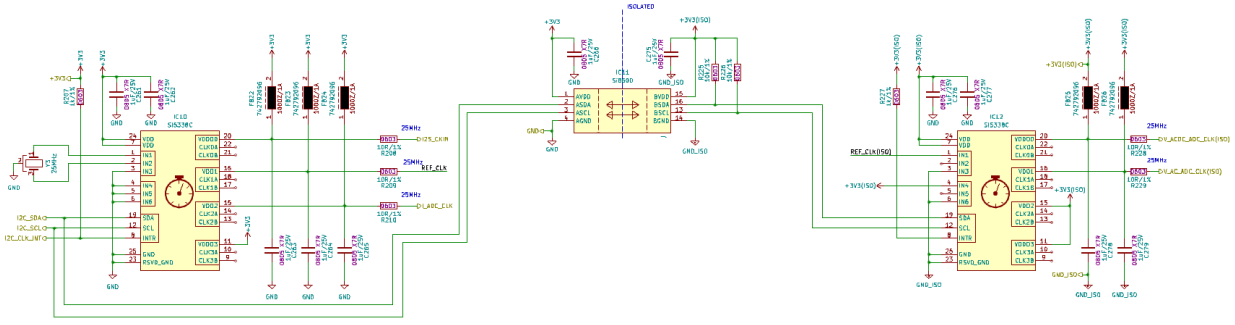


Figure 116: Circuit of the clock sources for operating the ADCs of the current measurement channel as well as the voltage measurement channel, source: own illustration.

[70] Cf. Skyworks Solutions, Inc (2021), Online-Source [11.3.2024] p. 13.

8.12.2 Filter configuration

The ADC features internally built-in filter functions that are associated with the oversampling ratio (OSR). For the application on the cell probe, two types of filters are recommended. On one hand, the wideband filter, which is suitable for evaluating AC signals[71], on the other hand, the SINC4 filter, which is more suitable for DC evaluation[72]. The filter configuration is performed via the SPI interface and is controlled by the microcontroller. Different data rates are enabled depending on the selected OSR. The relationship is evident for the wideband filter in Figure 117 and for the SINC4 filter in Figure 118.

OSR	DATA RATE (kSPS)	–0.1-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
32	400	165.000	10.6	108.7	19.5
64	200	82.500	7.47	111.8	20.1
128	100	41.250	5.20	114.9	20.6
256	50	20.625	3.66	118.0	21.1
512	25	10.312	2.58	121.0	21.6
1024	12.5	5.156	1.83	124.0	22.1
2048	6.25	2.578	1.29	127.0	22.6
4096	3.125	1.289	0.92	130.0	23.1

Figure 117: Wideband filter performance, source: Texas Instruments Incorporated (2022), Online-Source [31.9.2023] p. 26.

OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
12	1066.666	242.666	76.3	91.6	16.7
16	800	182.000	27.3	100.5	18.2
24	533.333	121.333	10.4	108.9	19.6
32	400	91.000	7.96	111.2	20.0
64	200	45.500	5.57	114.3	20.5
128	100	22.750	3.90	117.4	21.0
256	50	11.375	2.80	120.3	21.5
512	25	5.687	1.98	123.3	22.0
1024	12.5	2.844	1.40	126.3	22.5
2048	6.25	1.422	0.99	129.3	23.0
4096	3.125	0.711	0.70	132.3	23.5

Figure 118: SINC4 filter performance, source: Texas Instruments Incorporated (2022), Online-Source [31.9.2023] p. 27.

For use on the cell probe, an OSR (oversampling ratio) of 32 to 4098 is recommended for both the wideband filter and the SINC4 filter, depending on the signal frequency being examined.

[71] Cf. Texas Instruments Incorporated (2022), Online-Source [31.9.2023] p. 29.

[72] Cf. Texas Instruments Incorporated (2022), Online-Source [31.9.2023] p. 37.

8.12.3 SPI interface

All three ADCs are read out in parallel, which means that three SPI interfaces need to be implemented on the microcontroller side. Depending on the data rate setting, at least three sets of 24-bit data need to be read out simultaneously. With an OSR of 32, this means that 72 bits need to be read out 400,000 times per second, resulting in a data rate of 3.6 Mbps. The theoretically maximum achievable data rate depends on the performance of the microcontroller and the physical design of the PCB. The STM32H747 supports up to six SPI interfaces with a clock frequency of 150 MHz[73], which corresponds to a maximum achievable data rate of 18.75 Mbps.

8.12.4 Connection of the measurement channels to the ADC

By flipping the OUT+ and OUT- pins of the FDA to the INP+ and INP- pins of the ADC, a phase shift of 180° can be achieved. This allows measurement channels with an odd number of inverting op-amps to be balanced to an even number. The current measurement channel has a total of three OPVs and thus does not need to be flipped, for the voltage channel with DC decoupling as an example, which has four op-amps in its signal processing path. The voltage channel with single-stage amplification as well as the setting with tenfold amplification need to be flipped, as three op-amps are in series here.

8.12.5 Measurement quality of the ADCs

In this chapter, the measurement quality of the ADCs is evaluated for both the voltage channels and the current channel.

8.12.6 ADC resolution

The ADC has a resolution of 24 bits; however, noise must be considered, which affects the effective number of bits (ENOB). This entails accounting for the noise from analog signal processing and the intrinsic noise of the ADC due to semiconductor components. Consequently, the ENOB is calculated for each possible OSR in tabular form (Table 16 and Table 17). Subsequently, the final SNR is calculated.

It also considers to what extent the choice of input range influences the result. The input range can be configured via the SPI interface. This results in a Full-Scale Range (FSR) of 2 V_{ref} for single input range and 4 V_{ref} for double input range. The following equation(8.23) [74] applies for ENOB.

$$ENOB = \log_2\left(\frac{FSR}{e_n}\right) \quad (8.23)$$

$ENOB$ /Bit Enable number of bits

FSR Full scale range modus

e_n/V Noise voltage

[73] Cf. STMicroelectronics (2019), Online-Source [15.1.2024] p. 2.

[74] Cf. Texas Instruments Incorporated (2022), Online-Source [31.9.2023] p. 26.

OSR	e_n / μV_{RMS}	U_{n1x} / μV_{RMS}	U_{n10x} / μV_{RMS}	U_{nDC} / μV_{RMS}	U_{nI} / μV_{RMS}	$ENOB_{1x}$		$ENOB_{10x}$		$ENOB_{DC}$		$ENOB_I$	
32	10.6	11.728	14.394	13.281	12.535	17.77	18.77	17.61	18.61	17.67	18.67	17.72	18.72
64	7.47	11.728	14.394	13.281	12.535	17.99	18.99	17.87	18.80	17.87	18.87	17.93	18.93
128	5.2	11.728	14.394	13.281	12.535	18.17	19.17	18.04	18.96	18.04	19.04	18.10	19.10
256	3.66	11.728	14.394	13.281	12.535	18.31	19.31	18.17	19.07	18.17	19.17	18.23	19.23
512	2.58	11.728	14.394	13.281	12.535	18.41	19.41	18.26	19.16	18.26	19.26	18.33	19.33
1024	1.83	11.728	14.394	13.281	12.535	18.49	19.49	18.33	19.23	18.33	19.33	18.40	19.40
2048	1.29	11.728	14.394	13.281	12.535	18.55	19.55	18.38	19.28	18.38	19.38	18.46	19.46
4096	0.92	11.728	14.394	13.281	12.535	18.59	19.59	18.42	19.31	18.42	19.42	18.50	19.50

Table 16: Results when applying the wideband filter, source: self-created.

OSR	e_n / μV_{RMS}	U_{n1x} / μV_{RMS}	U_{n10x} / μV_{RMS}	U_{nDC} / μV_{RMS}	U_{nI} / μV_{RMS}	$ENOB_{1x}$		$ENOB_{10x}$		$ENOB_{DC}$		$ENOB_I$	
32	7.96	11.728	14.394	13.281	12.535	17.95	18.95	17.77	18.77	17.84	18.84	17.89	18.89
64	5.57	11.728	14.394	13.281	12.535	18.14	19.14	18.01	18.93	18.01	19.01	18.07	19.07
128	3.9	11.728	14.394	13.281	12.535	18.28	19.28	18.15	19.06	18.15	19.15	18.21	19.21
256	2.8	11.728	14.394	13.281	12.535	18.39	19.39	18.24	19.15	18.24	19.24	18.31	19.31
512	1.98	11.728	14.394	13.281	12.535	18.47	19.47	18.32	19.22	18.32	19.32	18.39	19.39
1024	1.4	11.728	14.394	13.281	12.535	18.53	19.53	18.37	19.27	18.37	19.37	18.45	19.45
2048	0.99	11.728	14.394	13.281	12.535	18.58	19.58	18.41	19.31	18.41	19.41	18.49	19.49
4096	0.77	11.728	14.394	13.281	12.535	18.61	19.61	18.44	19.33	18.44	19.44	18.52	19.52

Table 17: Results when applying the SINC4 filter, source: self-created.

The resolution of each channel is calculated as follows. With the 24-Bit resolution, the LSB value for a reference voltage of 2.5 V is 149.012 nV. In the configuration with double input range, the value doubles to 298 nV. When applied to the different current and voltage channels, the following values are obtained. Only values in the single input mode are provided. If the double input voltage mode is used, the minimum value doubles. These calculations are performed without noise influence.

For the "Voltage Channel with single-stage amplification," the smallest measurable voltage without noise influence is 400 times the LSB, which is approximately 59.6 µV/LSB in 1x Input mode and twice as much in 2x Input mode.

In the case of the tenfold amplification configuration, the minimum measurable voltage is 596.04 nV, obtained by 4 times the LSB, and likewise, it doubles in the case of the 2x input mode.

For the current measurement channels, the following resolutions can be achieved:

- For the 20 mA channel, a current-to-voltage ratio of 0.008 A/V results in an LSB value of 1.19 nA.
- For the 0.5 A, 1 A, and 2 A measurement ranges, current-to-voltage ratios of 0.2 A/V, 0.4 A/V, and 0.8 A/V respectively are obtained, resulting in LSB values of 29.8 nA, 59.6 nA, and 119.2 nA.
- For voltage-supplying current sensors, a resolution of 596.94 nA per LSB is obtained.

8.12.7 ADC SNR

From Table 16 and Table 17, it can be observed that when choosing the Wideband filter or the SINC4 filter, the minimum ENOB is 17 bits, 18 bits, and 19 bits, respectively. Thus, the specification regarding the minimum resolution is met. Whether this also applies to the SNR is being investigated. Quantization noise must also be considered, Since the excitation signal is sinusoidal, the following formula can be applied following Equation (8.24).

$$SNR_{ADC} = 1{,}76dB + ENOB \cdot 6{,}02dB \quad (8.24)$$

SNR_{ADC}/dB Signal-to-noise ratio after conversion

$ENOB$/Bit Enable number of bits

Normally, instead of the ENOB value, the number of bits of the ADC resolution is simply entered, but it has been shown that the noise of the analog circuitry, including the noise of the ADC itself, allows for only 17 bits in the worst-case scenario. Thus, an SNR value of 104.1 dB is obtained after analog-to-digital conversion. Therefore, the specification has been met because the SNR improves in the case of 18- and 19-Bit ENOB.

9 CALIBRATION CONCEPT

Since impedance is to be measured, it is important to ensure that gain error as well as phase shift error between the current measurement channel and the voltage measurement channel are corrected.

In general, impedance can be described as follows.

$$\underline{Z}_{CELL} = \frac{U_{MEA} \cdot e^{j\omega+\varphi_u}}{I_{MEA} \cdot e^{j\omega+\varphi_i}} \quad (9.1)$$

$\underline{Z}_{CELL}$/Ω Cell impedance

U_{MEA}/V Measured voltage

I_{MEA}/A Measured current

A difference in amplitude causes the measured current or voltage amplitude to appear larger or smaller than it actually is. A phase shift caused by the measurement circuit, for example, would lead to an incorrect conclusion about the capacitive component of the RC circuit. Therefore, these errors must be minimized through calibration as much as possible.

An example is implemented based on the results in section 4.2.3. There, at an amplitude of 1 A and a frequency of 10 kHz, a voltage of 54.9 mV is obtained. In this example, let's assume the measured current is 10 A at 10 kHz, which would result in a voltage of approximately 549 mV. This voltage is to be captured with the "Voltage Channel with DC Decoupling," while the measured current is measured using a voltage-supplying Fluxgate current sensor, which outputs a voltage of +/-10 V for +/-50 A at FS for AC/DC current measurements. This sensor is connected to the corresponding current measurement channel. Since the simulation corresponds to a galvanometric measurement, the measured current corresponds to the following equation.

$$\underline{I}_{MEA} = \frac{20\ A}{\sqrt{2}} \cdot e^{j\omega+\varphi_i} \quad (9.2)$$

The phase shift φ_i of the measured current is 0°, as the current represents the reference quantity. The measured voltage signal follows the following relationship.

$$\underline{U}_{MEA} = \frac{0{,}549\ V}{\sqrt{2}} \cdot e^{j\omega t+\varphi_u} \quad (9.3)$$

The simulation resulted in a phase shift from current to voltage of approximately 1.443 °. See Figure 119.

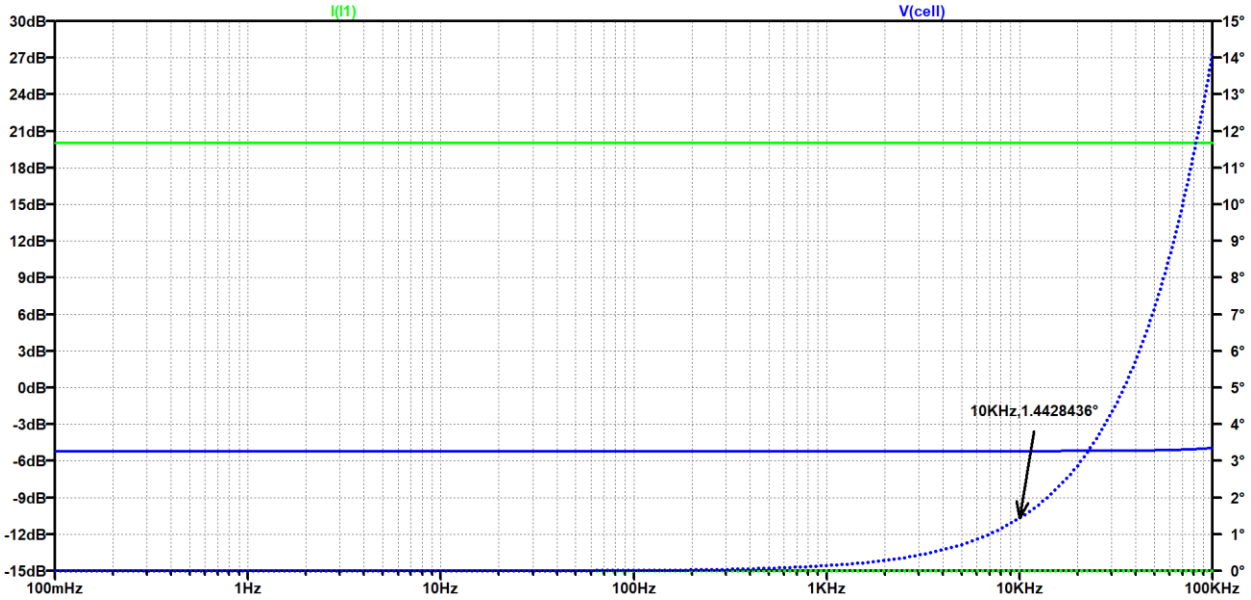


Figure 119:Results of the simulation circuit described under 4.2.3 p.17 The blue curve corresponds to the cell voltage, and the green curve represents the current through the cell. The measurement point of the phase at the 10 kHz position is marked, source: self-created.

The simulation shows that at 10 kHz, the inductance has a greater effect than the capacitance. From this, the following ideal result arises.

$$\underline{Z}_{CELL} = \frac{\frac{0{,}549\ V}{\sqrt{2}} \cdot e^{j\omega+1{,}443°}}{\frac{10\ A}{\sqrt{2}} \cdot e^{j\omega}} = 0{,}0549\ \Omega\ e^{+j1{,}443°}$$

Taking into account the phase shift added by the measurement channels, the following situation arises: The current channel exhibits a phase shift of approximately -24 ° relative to the reference, which corresponds to a positive angle of 336 °. For the voltage channel with DC decoupling, the phase shift is approximately -206 °, corresponding to a positive angle of 154 °. At 10 kHz, the phase shift generated by the impedance adds up to 155.443 °. Applying equation (9.1) yields a result where the angle is assumed to be positive: $Z_{cellMEA}$ = 0.0557Ω $e^{j\omega t}$ + 155.443 °.

Since the systematic measurement errors are known, the error in the impedance magnitude and phase shift can be corrected computationally. However, in reality, apart from component tolerances and ambient temperature, the physical design in the form of the PCB also contributes, meaning that an unknown error adds to the known systematic error. This can only be reduced through calibration. Four types of errors can be identified in this context.

- Offset error
- Channel gain error
- Voltage to current channel gain mismatch
- Voltage to current phase mismatch

Additional measurement errors such as the Integral Nonlinearity (INL) or Differential Nonlinearity (DNL) of the ADC are not considered in this work.

9.1.1 Offset error

Offset errors, for instance, arise from asymmetries in components and contribute to the measurement values. These can be corrected by applying a known voltage.

9.1.2 Channel gain error

Each current and voltage channel exhibits varying gains due to component tolerances, parasitic parameters, ambient temperature, and physical design. Similar to offset errors, these gains can be corrected by applying a known voltage. However, these gain errors are also frequency dependent. Therefore, in the calibration process, a known voltage or current amplitude must be applied at different frequencies to correct these errors.[75]

9.1.3 Voltage to current channel gain mismatch

As described in section 9.1.2, each channel has an unknown and likely different gain. This could lead to incorrect results, as it would result in different and unknown weighting of voltage and current.

9.1.4 Voltage to current phase mismatch

The differing gains, affected by component tolerances, ambient temperature, self-heating, and physical design, also influence the phase shift of each channel. A phase mismatch leads to errors in calculating the capacitive or inductive components of the impedance, resulting in incorrect fit values in the parameter fitting process during EIS post-processing. Similar to correcting channel gain, this error can be corrected, but the phase shift between the calibration signal and the measurement signal must be evaluated.[76]

[75] Translation assistance by ChatGPT.

[76] Translation assistance by ChatGPT.

9.1.5 Internal online self-calibration

On the Cell Probe, a self-calibration application called Internal Online Self-Calibration (IOSC) has been implemented. The IOSC is a continuous calibration method, meaning it can be implemented at any time. This implies that the warming up can be measured by the built-in temperature sensors. Therefore, the strategy would be to take the cell monitor with the cell probe in operation until the temperature stabilizes. Then, an initial IOSC is performed.[77] After that, regular measurements can commence, and the IOSC can be repeated at regular intervals.

It consists of three reference voltage sources and a DAC. However, before it can be used, the generated calibration signals need to be measured with a highly precise measuring device with a known measurement inaccuracy.

The schematic diagram (Figure 120) shows the calibration circuit of the current measurement channels. Two of the three reference voltage sources (REF1 and REF2) are connected in parallel to allow for a higher calibration current. Additionally, a reference shunt (Figure 120, R66) has been added. The calibration is controlled via IC8. The reference voltage sources can be activated and deactivated through the switches S1-D1 and S2-D2 via the SHDN! pin.

To correct the offset error and gain error, the reference voltage sources are activated, and 5V is applied through R66 to all shunts, except for the current measurement channel for voltage-supplying current sensors in series (see Figure 121, CAL_DC_HR signal). This allows for the correction of both offset and gain errors and the measurement of changes in the shunt resistances. The calibration voltage and the reference shunt R66 can be externally measured via the connector J8.

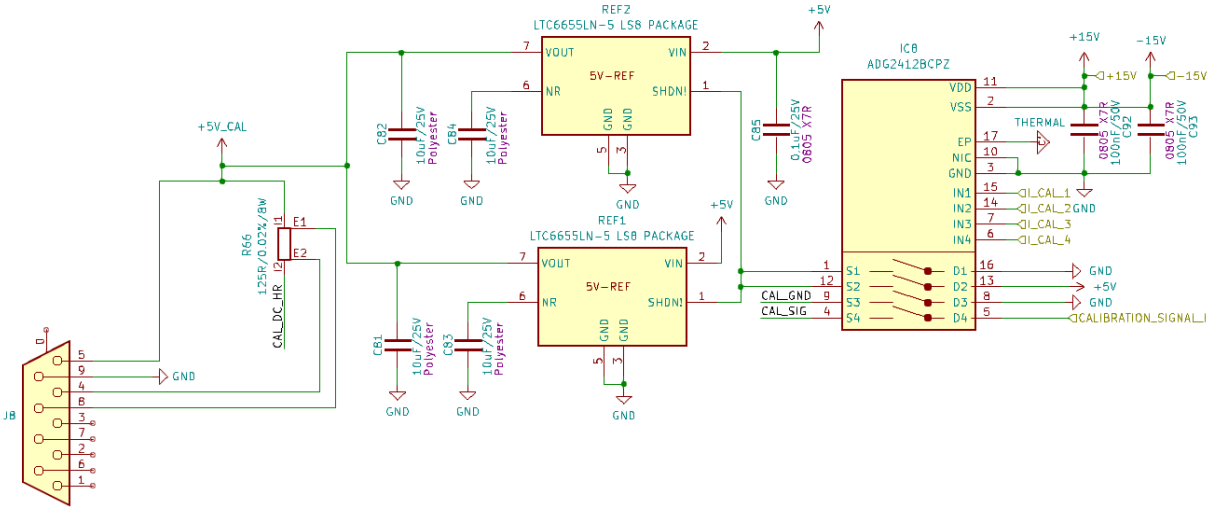


Figure 120: Calibration signal impression - calibration circuit for current measurement channels, source: own illustration.

[77] Translation assistance by ChatGPT.

Through the switch S4-D4 of IC8, the calibration signal generated by the DAC can also be applied to all shunts of the current measurement channels, including those for voltage-supplying sensors. By applying a signal with known amplitude, frequency, and phase, dynamic gain errors as well as mismatches in phase and amplitude relative to the voltage measurement channel can be corrected.

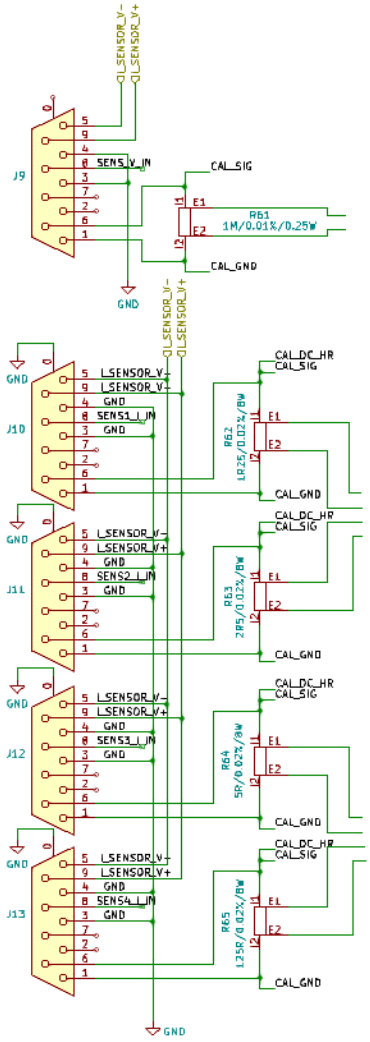


Figure 121: Circuit of the different current channels and their calibration connections, source: own illustration.

Calibration signals for the voltage measurement channel are impressed via the reed relays at the “voltage signal connector” block.

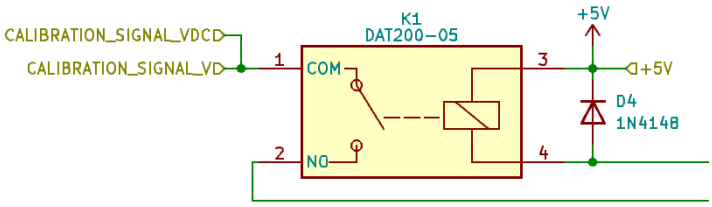


Figure 122: The calibration signals for the voltage measurement path are introduced differently, source: own illustration.

The DAC, along with its AIF generating the calibration signals, is housed together with the third 5 V voltage reference for the voltage measurement channel in the Calibration DAC circuit block. This circuit section has been enhanced with the addition of the 5 V reference to the existing schematic.

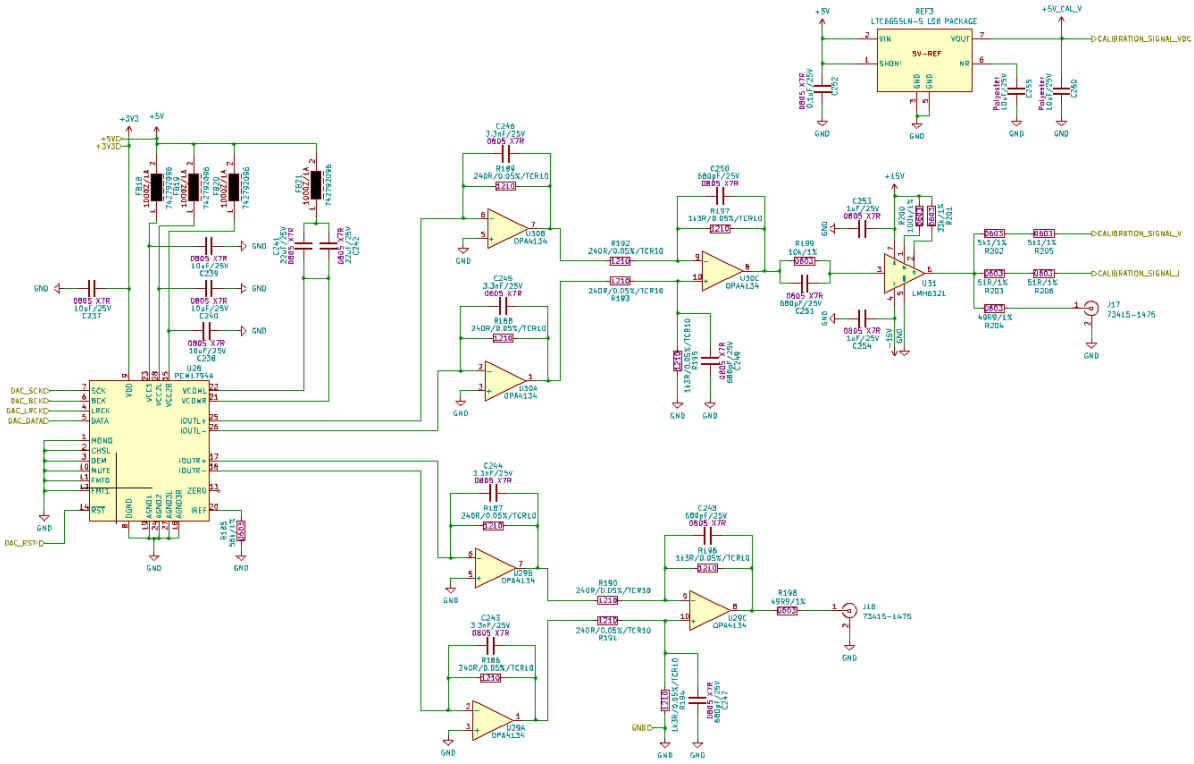


Figure 123: Schematic of der calibration DAC with 5 V reference, source: own illustration.

If the phase shift and the amplitude response of each channel are known, the phase mismatch and gain mismatch can be corrected by aligning them with each other. For the ISOC to deliver accurate results, it must also be calibrated.

9.1.6 General calibration

In the IOSC, changes in the reference sources and the shunt resistors of the high-voltage attenuator cannot be detected. Therefore, it is necessary to perform a comprehensive calibration both initially and periodically thereafter. A highly accurate signal source with known errors is connected to each measurement channel, and signals with different frequencies and amplitudes between 0 V and FS or 0 A and FS are impressed. Since all components are subject to physical and chemical changes, such as those described by aging phenomena, component parameters will change more significantly in the early stages of the lifecycle than towards the end of the lifecycle.

Taking the long-term drift of the 5 V reference voltage source as an example, it is evident that the long-term drift with respect to output voltage changes most significantly within the initial 1200 hours of operation. Factors such as ambient temperature and self-heating due to operational conditions also play a significant role in this drift phenomenon.

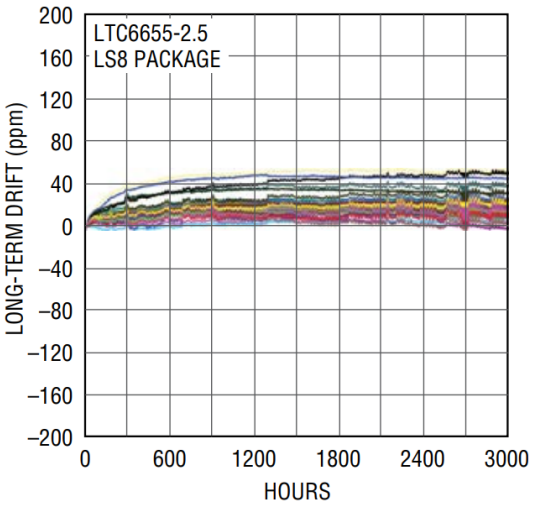


Figure 124: Long-Term drift of the LTC6655, ANALOG DEVICES, INC (21), Online-Source [20.4.2024] p.16.

This leads to two strategies for comprehensive calibration. One approach is to schedule calibration intervals with shorter periods, which are then reduced towards the end of the product's lifecycle. Alternatively, a so-called Burn-in test can be conducted, accelerating the physical and chemical alteration processes through increased stress. Consequently, the component parameters stabilize, and after the test, they undergo minimal further changes.

10 CONCLUSION

The revision of the cell monitor at the module level has expanded its capabilities. The more powerful SBC enables the execution of analysis software directly on the cell monitor, eliminating the need for post-processing by an external host PC in some applications. The additional GPIOs of the SBC allow for the implementation of additional measurement, control, and regulation measures in the form of additional hardware. Integrating a hard drive allows for the collection of measurement data over longer periods, which facilitates handling in applications such as automotive.

The revision of the power supply concept reduces wiring complexity through the use of switching voltage regulators. Additionally, the new current sensor supply provides enough power to operate a wide range of Fluxgate current sensors.

By revising and characterizing the voltage and current measurement channels, the measurement characteristics of the cell monitor can now be compared with other devices. It is observed that the channel with tenfold amplification exhibits poorer performance than expected. However, due to its advantage of AC decoupling in measurement operation, it is retained.

Expanding the current measurement channels allows for connection of various current-carrying sensors. The selection of shunt resistors avoids the need for a preamplifier for the ADC. The use of FDA in the MFB filter achieves common-mode rejection.

Regarding the anti-aliasing filter, further optimization could be achieved by slightly increasing the cutoff frequency to ensure minimal attenuation in the passband. The use of Delta-Sigma ADCs reduces the complexity of the anti-aliasing filter compared to SAR ADCs. Additionally, Fluxgate current sensors act as low-pass filters due to their frequency response.

The operating parameters of the ADC can be adjusted at any time via the SPI interface, increasing the flexibility of the cell monitor.

Expanding the calibration circuit allows for regular and user-friendly calibration of the cell monitor through ISOC, provided that basic calibration has been performed.

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LIST OF ILLUSTARTIONS

LIST OF TABLES

LIST OF ABBREVIATIONS

AC	Alternating current
ADC	Analog to digital converter
AEL	Alkaline electrolysis
CAN	Controller area network
CVM	Cell voltage monitoring
DAC	Digital-to-analog converter
DC	Direct current
DUT	Device under test
ECU	Electronic control unit
EDA	Electronic Design Automation
EIS	Electrochemical impedance spectroscopy
EL	Electrolyses
EMS	Institute for electrical measurement and signal analysis
FC	Fuel cell
FDA	Fully differential amplifier
GPIO	General purpose input/output
HER	hydrogen evolution reaction
HTEL	High temperature electrolyses
IOSC	Internal online self-calibration
LTI	linear time invariant system
MEA	Membrane electrode assembly
MFB	Multiple feedback
OC	Overcurrent
OCTH	Overcurrent threshold
OER	Oxygen evolution reaction
OV	Overvoltage
PEM	Proton exchange membrane
PEMFC	Polymer electrolyte membrane fuel cell
RC	Reverse current
SBC	Single board computer
SINAD	Signal-to-noise and distortion ratio
SPE	Solid polymer electrolysis
THD	Total harmonic distortion
UV	Undervoltage

APPENDIX

The circuit diagrams are located as attachments on the accompanying CD-ROM.